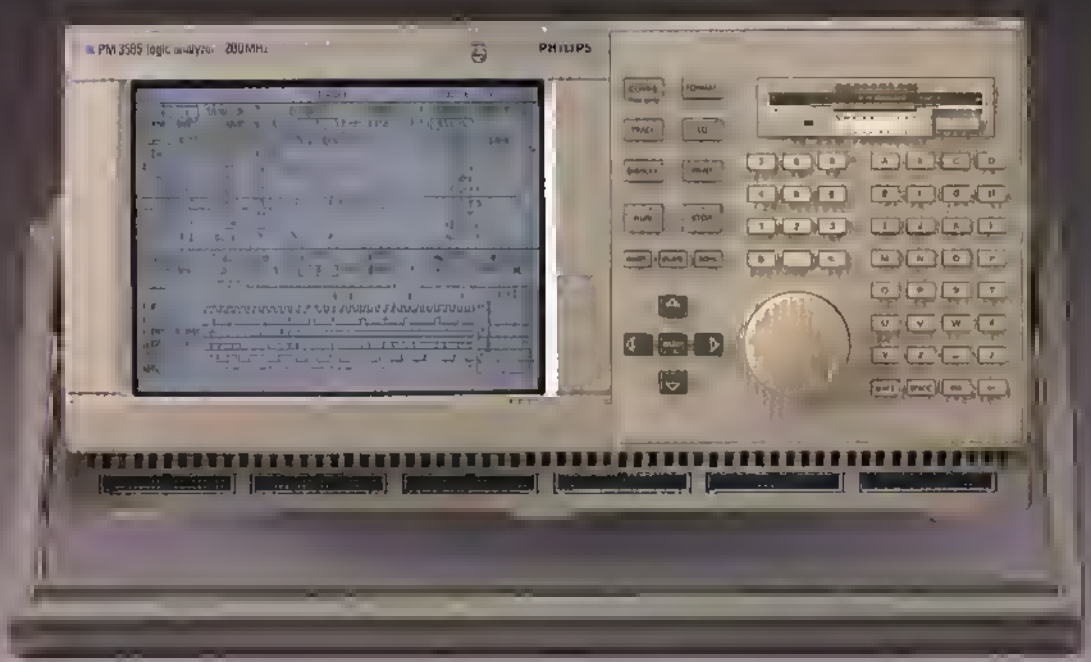
PHILIPS

LOGIC ANALYZERS PM 3580/PM 3585

Workshop Service Manual



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I. GENERAL.

I.1 GENERAL INFORMATION.

This manual contains all the information for completing installation, maintenance, calibration and servicing on the Logic Analyzers in the PM 3580/PM 3585 series.

Great care has been taken to ensure that all the information contained within this manual is complete and accurate. If, however, you find any omissions, or have any suggestions, please send your comments to the address below.

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INDUSTRIAL ELECTRONICS, T&M DIVISION
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I.2 GUARANTEE STATEMENT.

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Philips guarantees this product to be free from defects in material and workmanship under normal use and service for a period of one (1) year from the date of shipment. This guarantee does not cover possible required re-calibration and/or standard maintenance actions. This guarantee extends only to the original purchaser and does not apply to fuses batteries or to any product or part thereof that has been misused, altered or has been subjected to abnormal conditions of operation and handling.

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I.3 SAFETY INSTRUCTIONS.

Read these pages carefully before installation and use of the instrument.

INTRODUCTION

The following clauses contain information, cautions and warnings which must be followed to ensure safe operation and to retain the instrument in a safe condition.
Adjustment, maintenance and repair of the instrument must only be carried out by qualified personnel.

SAFETY PRECAUTIONS

For the correct and safe use of this instrument it is essential that both operating and service personnel follow generally-accepted safety procedures in addition to the safety precautions specified in this manual.
Specific warning and caution statements, where they apply, will be found throughout the manual. Where necessary, the warning and caution statements and/or symbols are marked on the apparatus.

CAUTION AND WARNING STATEMENTS

CAUTION: **IS USED TO INDICATE THE CORRECT OPERATION AND MAINTENANCE PROCEDURES IN ORDER TO PREVENT DAMAGE TO OR DESTRUCTION OF THE EQUIPMENT OR OTHER PROPERTY.**

WARNING: **CALLS ATTENTION TO A POTENTIAL DANGER THAT REQUIRES CORRECT PROCEDURES OR PRACTICES IN ORDER TO PREVENT PERSONAL INJURY.**

SYMBOLS

High Voltage (red) ≥ 1000V

Live Part (black/yellow)

Read the operating instructions

Protective earth (grounding) terminal

I.4 IMPAIRED SAFETY PROTECTION.

Whenever it is likely that safety-protection has been impaired, the instrument must be made inoperative and be secured against unintentional operation. The matter should then be referred to qualified technicians.

Safety protection is likely to be impaired if, for example, the instrument fails to perform the intended measurements or shows visible damage.

I.5 GENERAL CLAUSES.

WARNING: THE OPENING OF COVERS OR THE REMOVAL OF PARTS, EXCEPT THOSE TO WHICH ACCESS CAN BE GAINED BY HAND, IS LIKELY TO EXPOSE LIVE PARTS AND ACCESSIBLE TERMINALS WHICH CAN BE DANGEROUS TO LIFE.

- The instrument must be disconnected from all voltage sources before it is opened.
- Note that capacitors inside the instrument can hold their charge even if the instrument has been disconnected from all voltage sources.
- Components that are Important for the safety of the instrument may only be renewed by components obtained through your local Philips organisation.
- After repair and maintenance in the primary circuit safety inspection and tests must be carried out.
- All of the screws that are used to fix the system board to the frame of the logic analyzer must be in place at the completion of servicing as they have an effect on the EMC of the instrument.
- Before any connection to the input connectors is made, the instrument must be connected to a protective earth conductor via the three-core mains cable; the mains plug must only be connected to a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord without protective conductor.

WARNING: ANY INTERRUPTION OF THE PROTECTION EARTH CONNECTOR INSIDE OR OUTSIDE THE INSTRUMENT OR THE DISCONNECTION OF THE PROTECTION EARTH TERMINAL IS LIKELY TO MAKE THE INSTRUMENT DANGEROUS. INTENTIONAL INTERRUPTION IS PROHIBITED.

BEFORE CONNECTING THE EQUIPMENT TO THE MAINS OF THE BUILDING INSTALLATION, THE PROPER FUNCTIONING OF THE PROTECTIVE EARTH LEAD OF THE BUILDING INSTALLATION NEEDS TO BE VERIFIED.

LIST OF CHAPTERS.

LIST OF FIGURES.

NOTE: Words printed in ***{bold; italic}*** are stated in the Index in the back of this manual.

CHAPTER 1.

1. INTRODUCTION.

CONTENTS.

1.1 SYSTEM CONFIGURATION.

The PM 3580/PM 3585 family of logic analyzers are State and Timing Logic Analyzers for use within the R & D, Manufacturing, Service and Education environments. They are available in 32/64/96 channel models. The operating speed of the PM 3580 is 100 MHz and the operating speed of the PM 3585 is 200 MHz.

The PM 3580 and the PM 3585 each come in two ***basic models***, these are:

- PM 3580/30 32 dual analysis channels with 100 MHz Timing, 50 MHz state and 1K deep acquisition memory.
- PM 3580/60 64 dual analysis channels with 100 MHz Timing, 50 MHz state and 1K deep acquisition memory.
- PM 3585/60 64 dual analysis channels with 200 MHz Timing, 50 MHz state and 2K deep acquisition memory.
- PM 3585/90 96 dual analysis channels with 200 MHz Timing, 50 MHz state and 2K deep acquisition memory.

All of the above models have the following ***standard features***:

- Human interface of an integral keypad and rotary knob, and a nine inch white phosphor, high resolution CRT.
- 3.5 inch micro floppy disc drive for setup, storage and retrieval of data.
- Rear mounted BNC connections for input and output of trigger signals.
- External video port.
- Centronics printer interface.
- RS-232-C ports for other peripherals to be connected, e.g. a printer.
- Data acquisition is via any or all of the six inputs on the front of the unit.

The system assembly board centres on the 68070 16/32 bit CPU. It is accompanied by powerful data acquisition ASIC's that analyze the data received from the target system. An interface is used to ensure that the acquisition system is fully compatible with that of the CPU architecture. The system assembly board also contains the circuitry required to interface with the keyboard, disk drive, the CRT and the output ports.

1.2 PERIPHERAL EQUIPMENT.

The following ***accessories*** are available for the PM 3580 and the PM 3585 series of Logic Analyzers.

PF 8600/20	16 Channel logic pod.
PF 8600/21	16 Channel pod cable for PM 358X.
PF 8600/24	Gray, low profile, mini measuring clips.
PF 8666/20	Front cover with integrated acessory pouch.
PF 8669/20	Logic target.
PM 8819/30	50 Mini-measuring clips, red/dual pin.
PM 8902/00	12V DC/AC converter.
PM 8902/10	Mounting kit for PM 8902/00.
TC 100	Cart for PM 3580 or PM 3585 with two shelves.

NOTES.

CHAPTER 2.

2. INSTALLATION AND DISMANTLING.

CONTENTS.

2.1 GENERAL INFORMATION.

This section provides the ***dismantling procedures*** required for the removal of units and components during repair operations. Installation is the reverse procedure of the dismantling described below.

All items removed from the instrument must be adequately protected against damage, and should be put in a safe place. All normal precautions regarding the use of tools must be observed.

During dismantling a caretul note must be made of all leads that have to be disconnected so that they can be reconnected to their correct terminals during re-assembly.

CAUTION: Damage may result it:

- **The instrument is switched on when a unit has been removed or disconnected.**
- **A unit is removed within one minute of the instrument being switched off.**

2.1.1 SAFETY NOTICE.

The opening of covers or the removal of parts, except those to which access can be gained by hand, is likely to expose live parts, note also that accessible terminals may be live.

The instrument must be disconnected from all voltage sources before any adjustment, replacement or maintenance which requires the instrument to be opened.
Any adjustment, maintenance or repair of the instrument that has to be completed while the instrument is under voltage must only be carried out by a skilled person aware of the hazards involved.

The replacement of the mains plug is at the users risk, after a mains plug has been replaced a high voltage test in accordance with IEC publication 348 is strongly recommended.

Ensure that the instrument is set to the local mains voltage before inserting the plug into the mains socket.

Note that capacitors inside the instrument may still be charged even if it has been separated from all voltage sources. Use safety glasses and protective gloves when handling the CRT.

2.1.2 REQUIRED TOOLS AND MATERIALS.

For the complete disassembly of the instrument the following ***tools*** are required:

- Torx screwdrivers

SIZE		Concern Service code number
T8	-	4822 395 50263
T10	-	5322 395 50381
T20	-	5322 395 50418

- Flat blade screwdriver (small)

If the nylon tie wraps have been cut away from the internal wiring it is recommended that the wiring is fixed with new ties, service ordering code 5322 401 14154 (per item).

In order to avoid the loss of screws, nuts etc it is good practice to replace them in their original location, if possible, whilst the units are laying apart.

2.2 MAINS VOLTAGE SETTING.

The mains voltage of the instrument is set in the factory and is customised to the requirements of the country of destination. This setting can be changed using the following procedure, the two available settings being those of 110V and 220V.

- Disconnect the mains supply from the instrument.
- Prise the ***voltage selector*** unit (1) from the rear of the instrument.
- Lift the retaining lug that holds the voltage selector (2) into the unit and then remove the selector.
- Rotate the voltage selector so that the required figure will be displayed in the window of the unit and then replace the complete unit in the reverse order of that of the removal procedure.

NOTE: The correct fuse should be used for each of the voltage settings. The recommended fuse sizes are 2A slow for the 220V setting and 4A slow for the 110V setting.

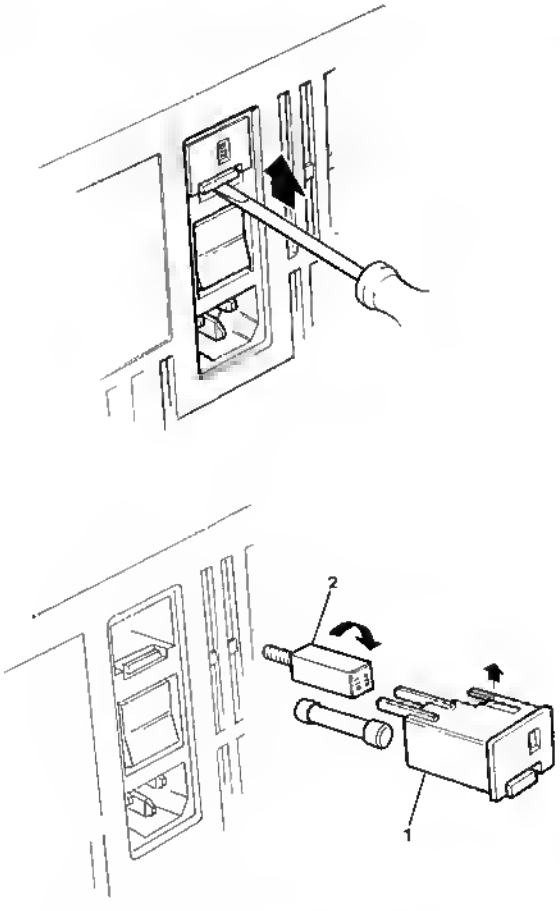


Fig. 2.1. The voltage selector assembly.

2.3 ACCESS TO PARTS.

Before commencing the removal of any cover or module of this instrument ensure that it has been disconnected from the main voltage supply. Remove any other external connections to the instrument.

2.3.1 REAR ACCESS PLATE.

- Ensure that all external connections to the instrument have been removed.
- Remove the brightness control knob (1) located in the bottom right corner of the rear plate by pulling it away from the spindle.
- Locate and loosen the two Torx screws (2) and washers on the rear cover.
- Remove the rear plate from the unit.

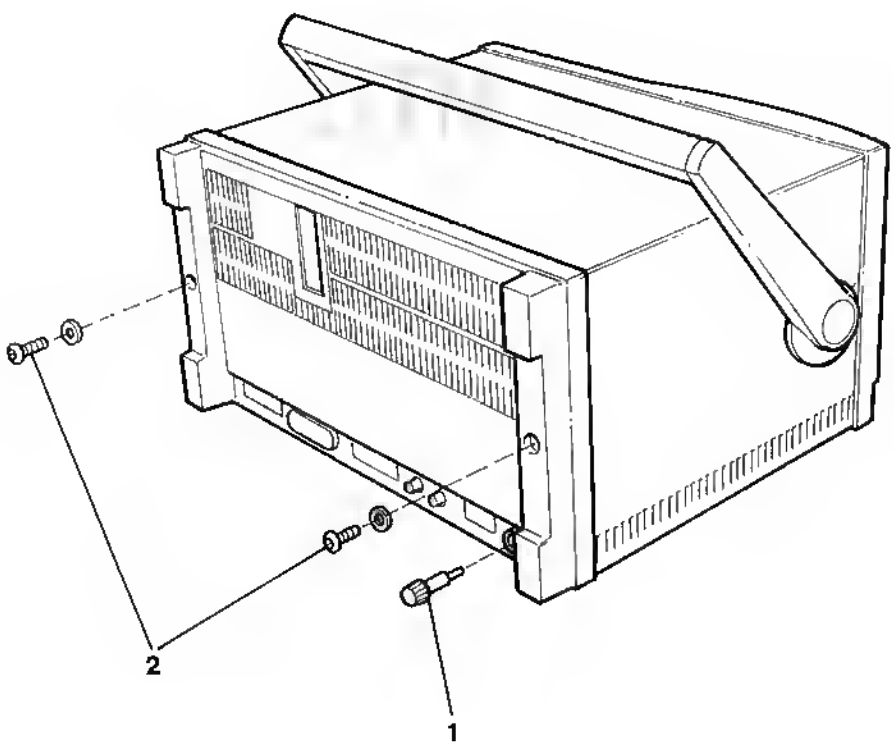


Fig. 2.2. The rear plate assembly.

2.3.2 INSTRUMENT SLEEVE.

- Complete procedure 2.3.1.
- Adjust the position of the ***carrying handle*** so that it is not obscuring the front of the instrument. (The position of the handle is altered by applying pressure to the centre of handle pivots and then moving the handle.)
- Position the instrument face down on the work surface using a piece of foam rubber (1), or similar material, to prevent the keyboard dial from touching the surface.
- Slide the sleeve (2) of the instrument away from the chassis.

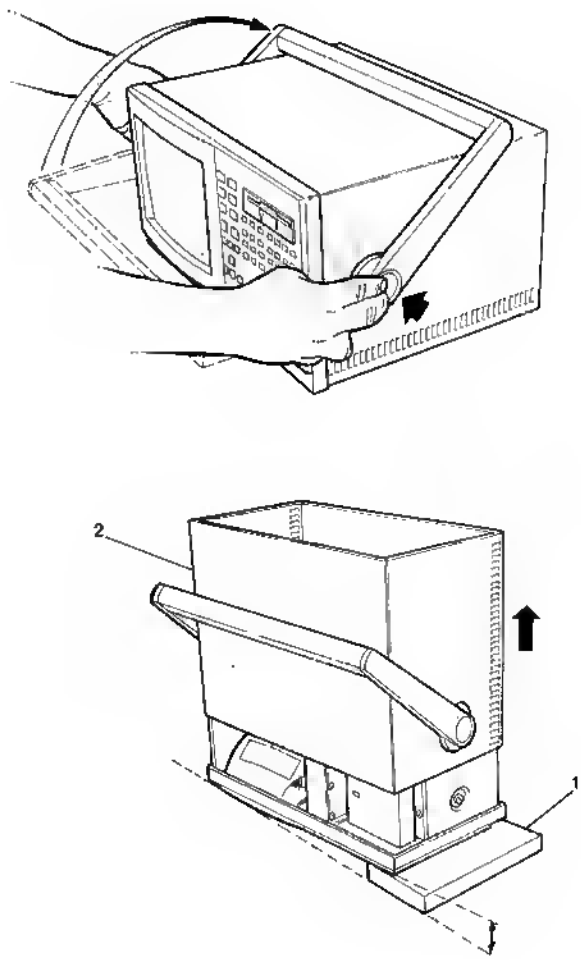


Fig. 2.3. The sleeve assembly.

2.3.3 HANDLE.

- Complete procedure 2.3.2.
- Insert a small blade into the slot in the central cover (1) of the handle pivot and prise off, this will reveal a slotted screw (2). Repeat this procedure for the other side of the handle.
- Remove the slotted screws (2) and washers (3) located on either side of the handle that fasten the handle to the instrument sleeve.
- Remove the handle assembly parts (4-8). It is suggested that you reassemble all the component parts of the handle pivot assembly to avoid misplacing them.

NOTE: Item 6 (stop disk) can be ordered separately at Concern Service. Code 5322 466 92997.
Item 4 (Handle side cover) can be ordered separately at Concern Service. Code 5322 600 30047.

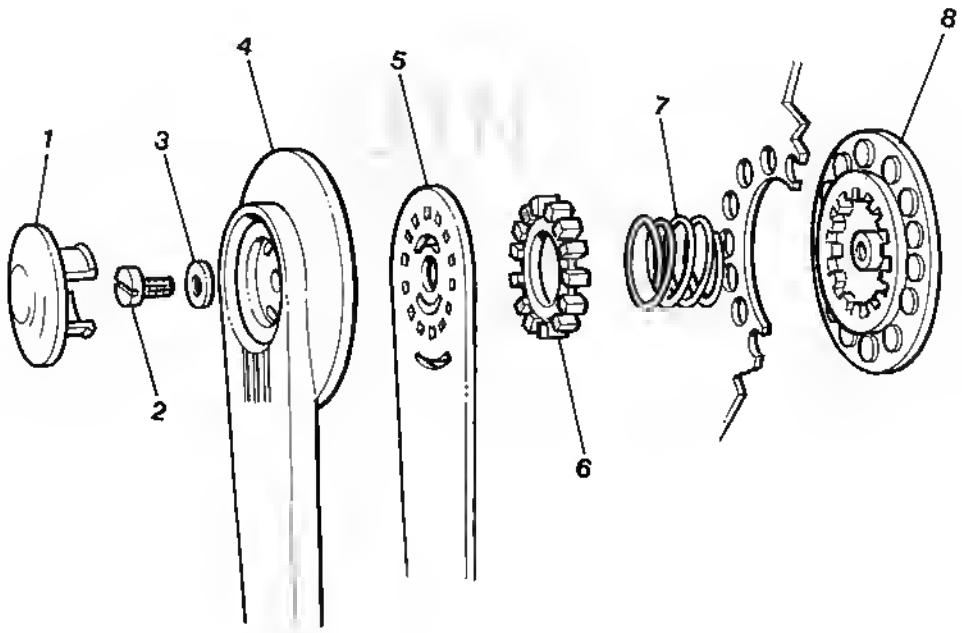


Fig. 2.4. Assembly of the handle.

2.3.4 DISK DRIVE ASSEMBLY.

- Complete procedure 2.3.2.
- Disconnect the power cable and ribbon cable attached to the rear of the disk drive.
- Remove the two screws (1) that fasten the disk drive, via grommets located in the bracket, to the cover of the power supply unit.
- If the bracket also has to be removed, remove the two screws (2) that fasten it to the power supply unit cover.
- Remove the disk drive by carefully lifting the rear of the drive so that it is able to clear the bracket and PCB and then gently pull it out of the instrument.
- Remove the disk drive from the mounting bracket by removing the four screws on the underside of the assembly.

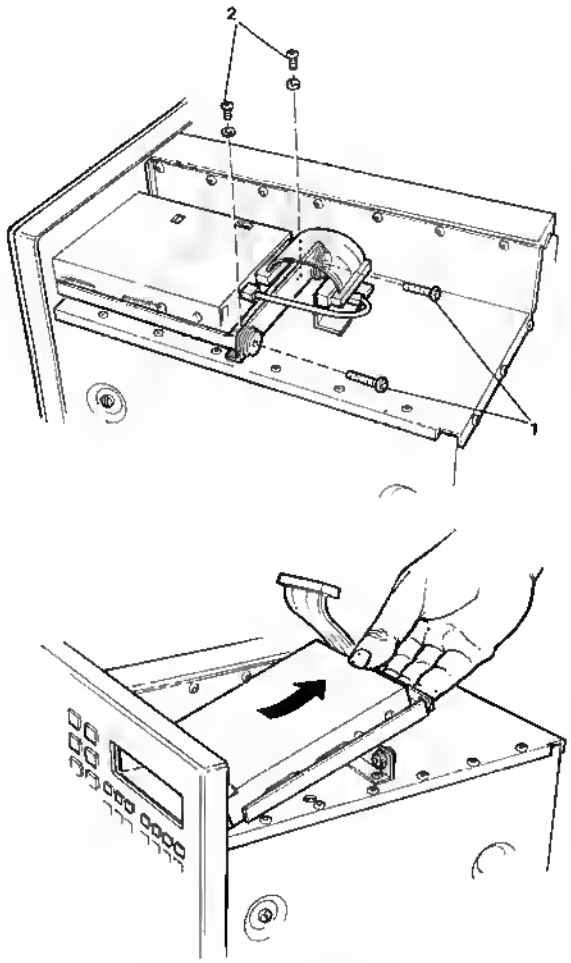


Fig. 2.5. Disk drive assembly.

2.3.5 KEYBOARD ASSEMBLY.

- Complete procedure 2.3.4.
- Gently press the fixing lugs (1) that attach the keyboard to the main fascia of the instrument so as to enable it to move.
- Pull the left hand edge of the keyboard toward you and withdraw the pad in the direction of the VDU screen, so as to free the three locating lugs (2).
- Disconnect the four wired plug that is attached to the keyboard.

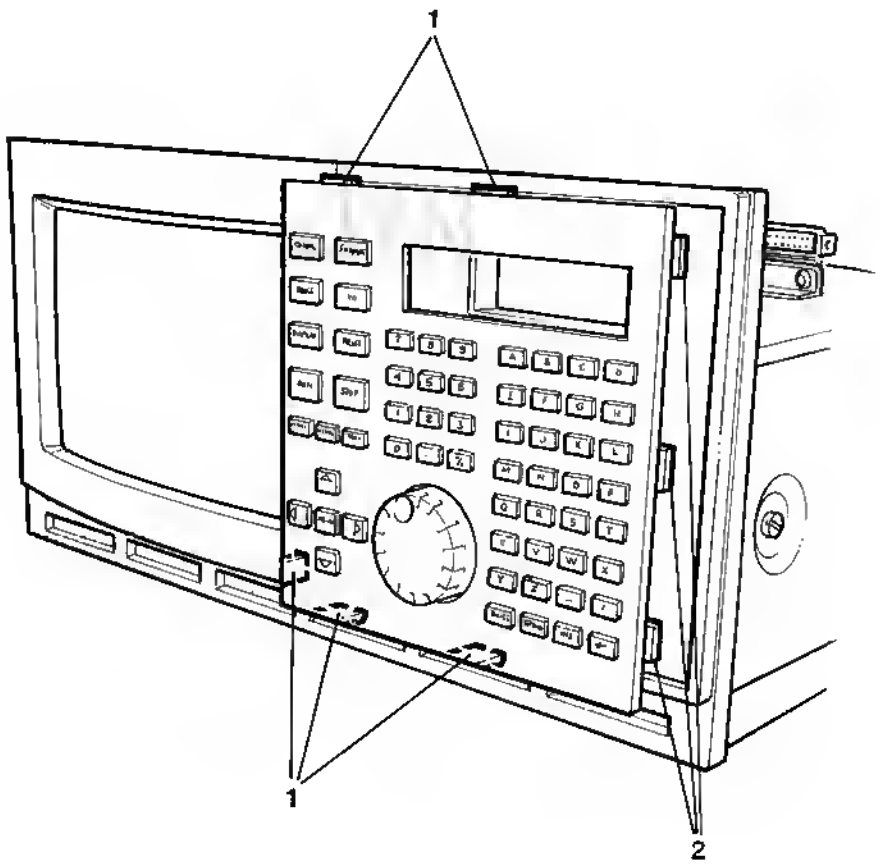


Fig. 2.6. Keyboard assembly.

2.3.6 MAIN BOARD ASSEMBLY.

- Complete procedure 2.3.2.
- Position the instrument so that it is upside down with the rear towards you.
- Remove the Torx screws that fasten the metal base plate to the printed circuit board. This will reveal the underside of the printed circuit board.

CAUTION **When re-assembling the instrument all of the Torx screws that have just been removed must be replaced. Failure to do so will severely affect the operation of the instrument.**

- Remove the Torx screws that fasten the rear metal bracket to the main chassis of the instrument.
- Lift the board towards you and gently pull it away from the chassis. Disconnect the three ribbon (1) and two power supply connectors (2) from the board and then continue withdrawing the board.

NOTE: There are twelve IC's located at the front of this board and care must be taken to avoid them being damaged during the removal procedure.

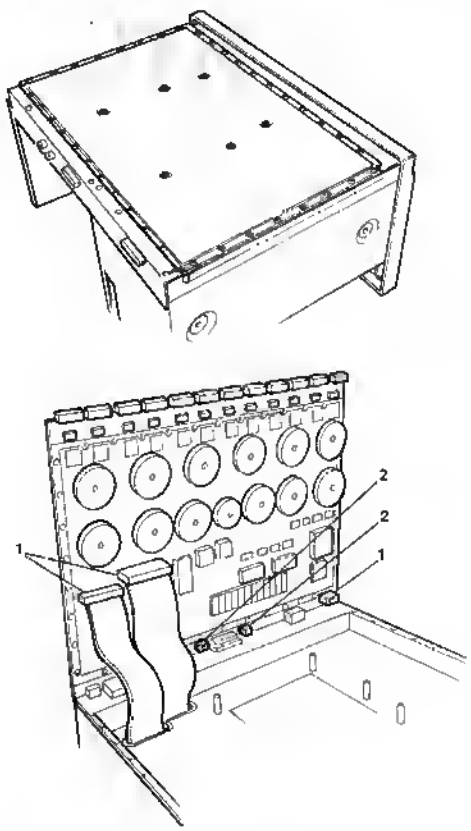


Fig. 2.7. Main board assembly.

2.3.7 POWER SUPPLY UNIT ASSEMBLY.

- Complete procedure 2.3.4.
- Remove all the Torx screws that fasten the PSU cover to the main chassis of the equipment.
- Disconnect the ribbon cable from the PSU cover.
- Remove the two screws (1) that fasten the mains input socket (2) to the chassis.
- Disconnect the two grounding wires (3) from their respective connectors on the mains input socket and the chassis.
- Disconnect the four wires (4) to the mains input socket, noting their positions and colours for correct reconnection.
- Lift the rear of the PSU circuit board up slightly and then remove the board from the chassis.
- Disconnect the ribbon cable from the front of the PSU.

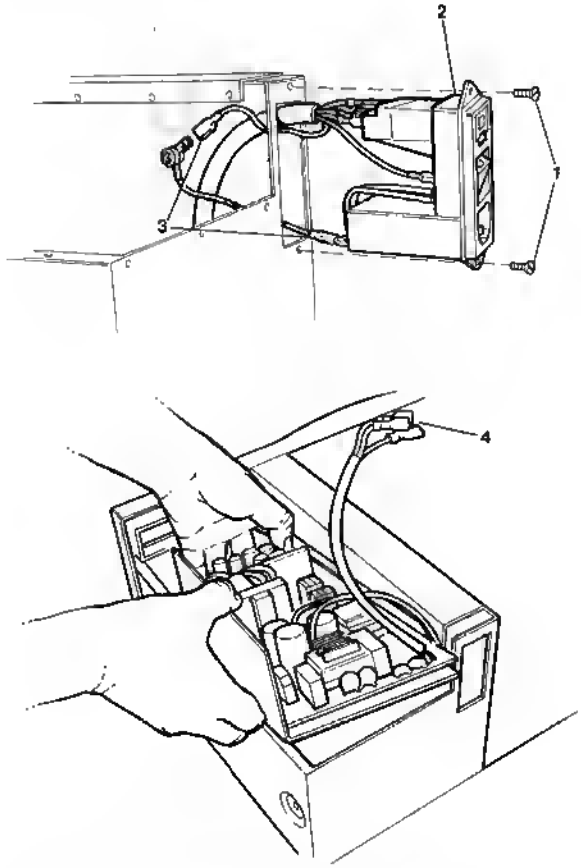


Fig. 2.8. Power supply unit assembly.

2.3.8 FAN UNIT ASSEMBLY.

- Complete procedure 2.3.2.
- Disconnect the fan unit power supply cable (1) from the socket on the chassis.
- Remove the Torx screws (2) that fasten the fan unit (3) to the instrument chassis.
- Lift the fan unit out of the instrument chassis.

WARNING: TAKE CARE NOT TO DAMAGE THE REAR OF THE CRT SO AS TO AVOID ANY RISK OF IMPLOSION.

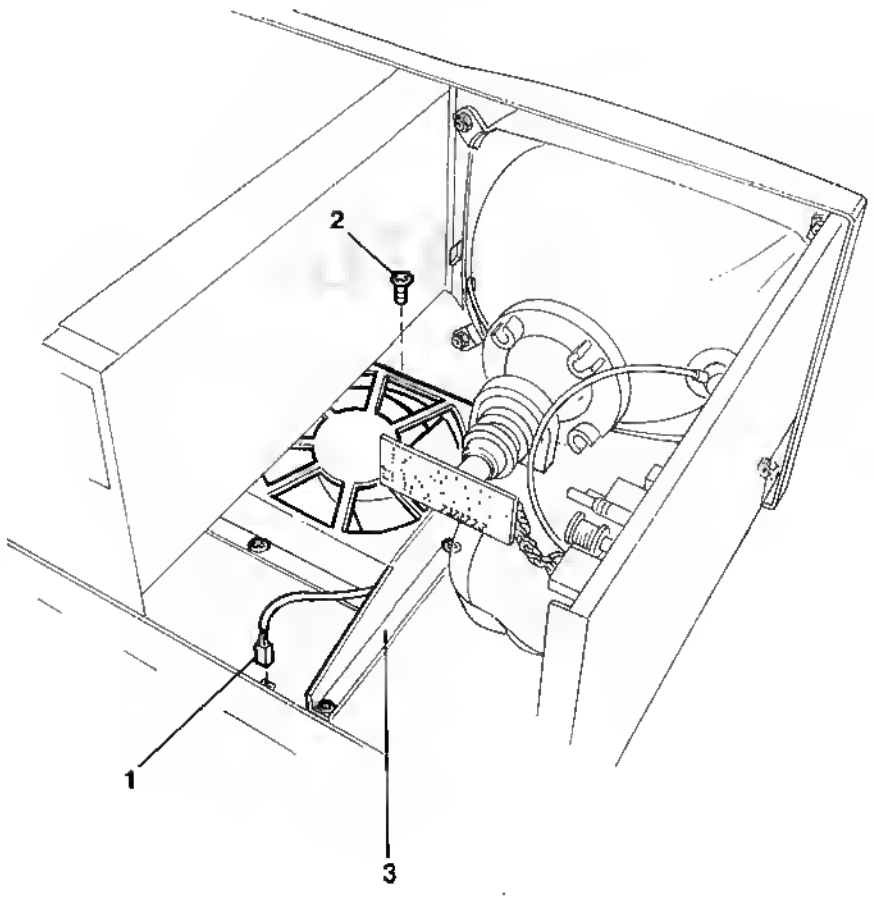


Fig. 2.9. Fan unit assembly.

2.3.9 VISUAL DISPLAY UNIT ASSEMBLY.

WARNING: BEFORE COMMENCING ANY TASK ON THE VDU ENSURE THAT THE CRT AND THE EHT CABLE HAVE BEEN DISCHARGED.

2.3.9.1 Assembly of PCB's

- Disconnect the two cables (2, 4) from the PCB and the EHT lead (1) from the CRT.
- Remove the grounding wire (5) from the CRT PCB and then pull this PCB away from the tube.
- Remove the five screws that fasten the PCB (3) to the chassis.
- Place the boards to one side.

2.3.9.2 Assembly of CRT

- Remove the CRT PCB and EHT lead (1).
- Undo the four locknuts that fix the CRT mounting bracket to the chassis of the instrument, being sure to support the CRT at all times. Note that one of the screws is slightly obscured by the fan unit, you may find it easier to complete procedure 2.3.8 before removing the CRT.
- Place the CRT (6) on a scratch free surface.

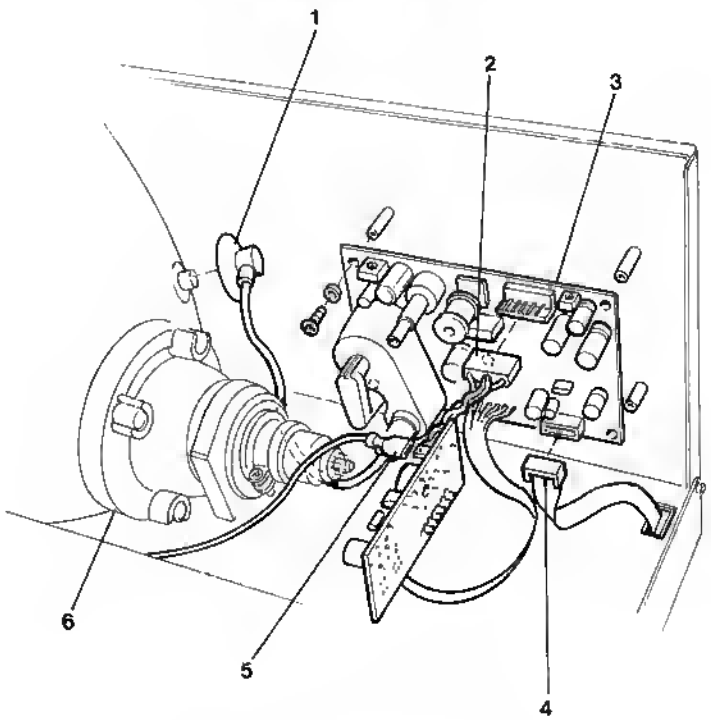


Fig. 2.10. VDU assembly.

NOTES.

CHAPTER 3.

3. MAINFRAME.

CONTENTS

3.1 GENERAL INTRODUCTION.

The mainframe of the Logic Analyzer comprises:

- Power Supply
- Floppy Disk Drive
- Keyboard
- Video Monitor
- Fan Unit
- Main Board

Each of these units will be described in this section.

3.2 POWER SUPPLY.

The switch mode power supply in the Analyzer supplies 3 output voltages i.e.

+ 5V / 20A
+12V / 2A
- 5V / 3A

Usage of the D.C. supplies:

+ 5V : by main-board, keyboard and floppy drive.
+12V : by monitor and fan unit
- 5V : by main-board

The power supply unit has several protection features:

1) The ***mains fuse*** for over-current protection in the primary stage (2A slow type for 220V and 4A slow type for 110V).
2) An over-current sense for the +5V.
3) Over-voltage protection's on -5V and +5V.
4) Over-current protection for +12V and -5V.
5) Thermal sense on heatsinks and externally controllable shutdown input.

If by accident a short circuit is made internally or at the POD input connectors (+5V or -5V shorted to ground), then the Analyzer should be switched off for at least 30 seconds. All output voltages of the power supply will again be available at the next switch on.

CAUTION: **ALWAYS USE A SEPARATION TRANSFORMER DURING MEASUREMENTS ON THE POWER SUPPLY. THIS IS NOT ONLY MUCH SAFER BUT ALSO PREVENTS EARTHED TOOLS OR EQUIPMENT FROM BEING SHORTED TO LIVE VOLTAGES.**

NOTE: For an Unit Drawing of the power supply refer to Fig. 4.1. of Chapter 4.

3.2.1 Block Diagram description.

The power supply is of the switched mode type.
The primary rectified mains voltage is chopped by the chopper transistors according to the power desired in the secondary circuit.

The chopper transformer transports the necessary amount of energy to the secondary circuit.
The chopper transistors are controlled by the pulse width modulator (PWM) circuitry. This PWM will increase the pulse width as soon as the load in the secondary circuit increases and vice versa.
In this way the output voltages are stabilized.
As soon as an emergency situation is sensed (short circuit, over voltage, over-current or overheating) the safety protection circuit will immediately shut down the PWM and by this the chopper stage.
Thus the output voltage's of the secondary circuit are switched off.

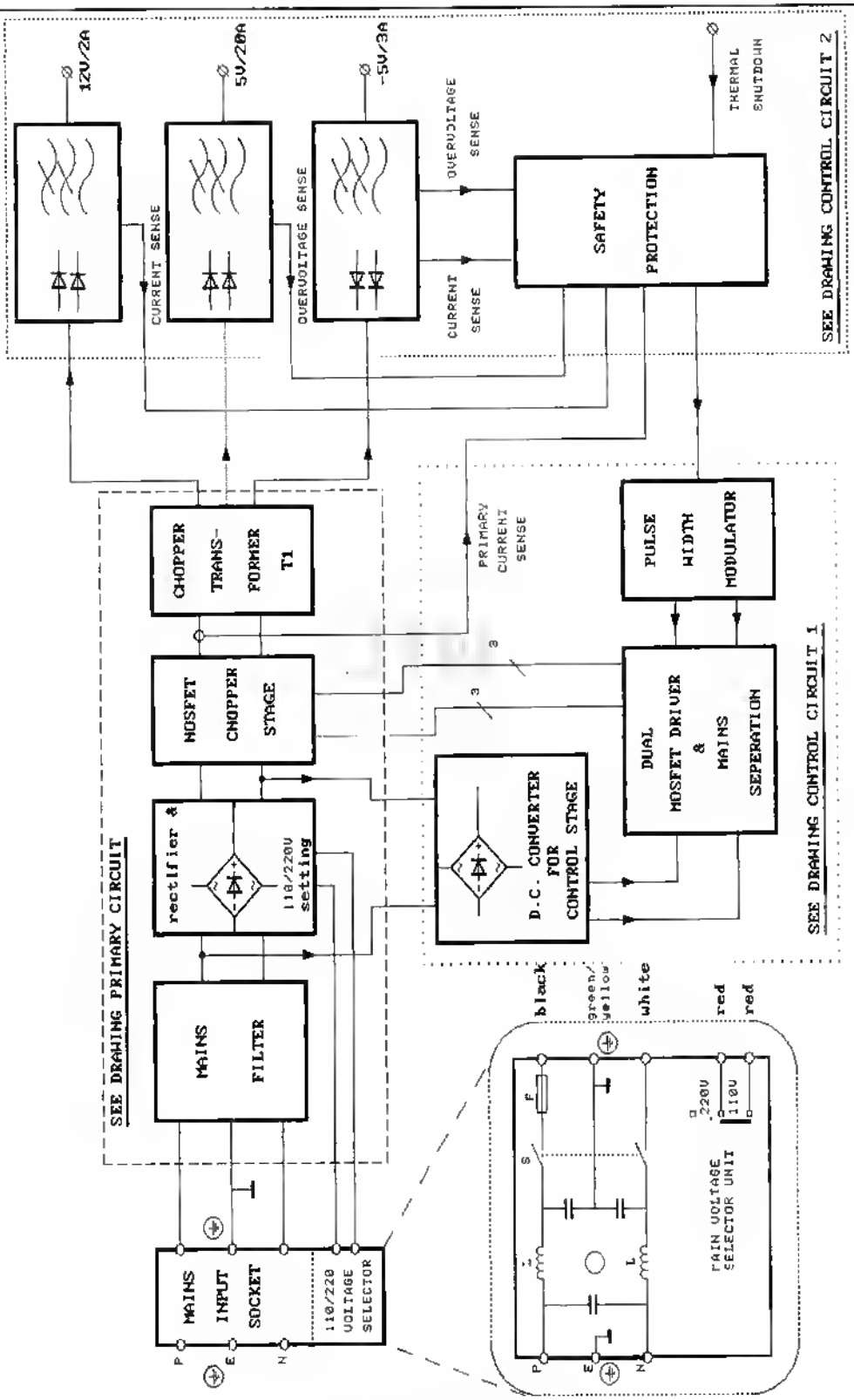


Fig. 3.1. Block diagram power supply.

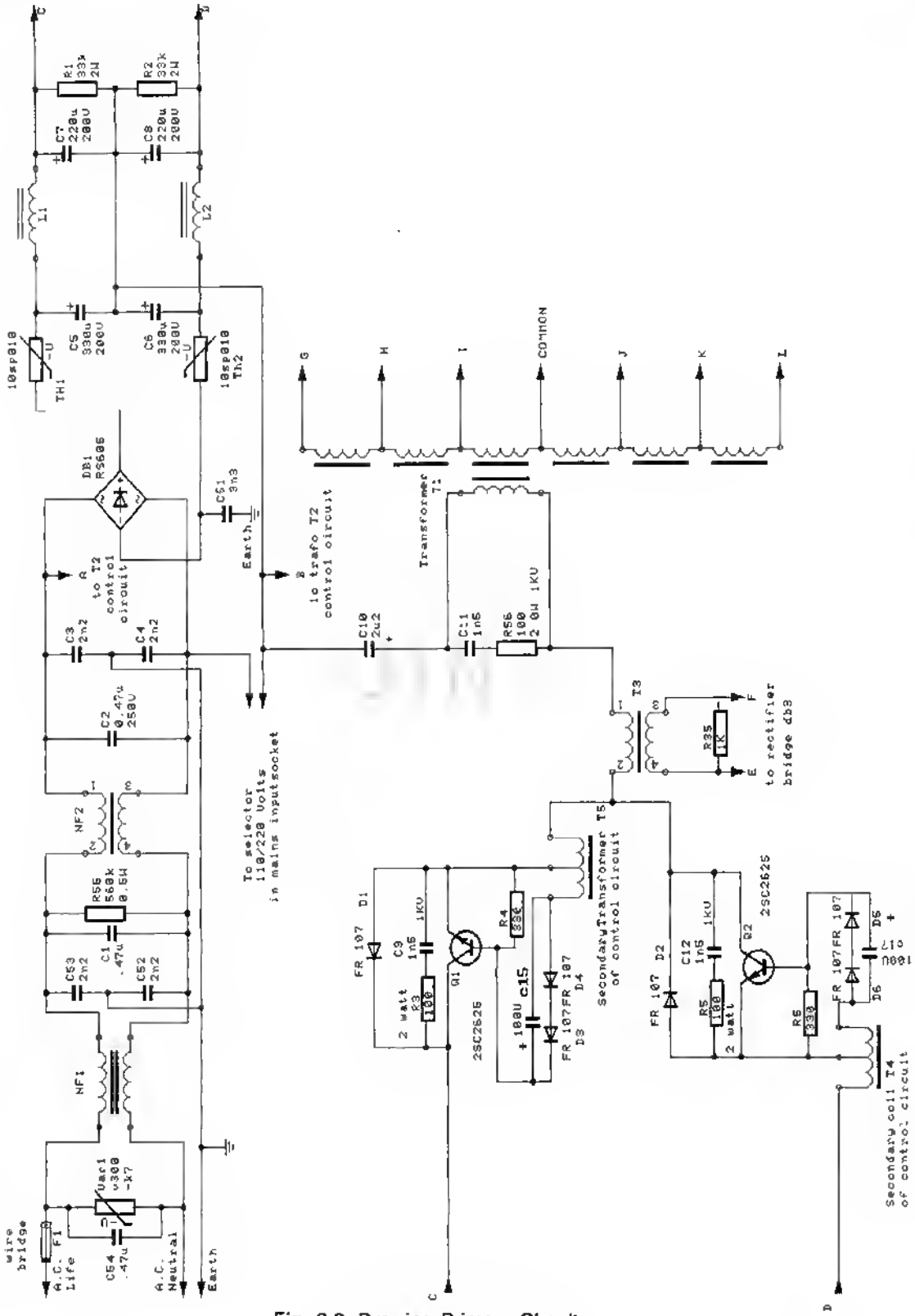


Fig. 3.2. Drawing Primary Circuit.

3.2.2 Circuit description.

3.2.2.1 The primary circuit.

The mains voltage is filtered by coils NF1 and NF2 as well as capacitors C1, C2, C3, C4, C52 and C53.
This voltage is rectified by rectifier bridge DB1.
The inrush current suppressors TH1 and TH2 protect the input circuitry against too high inrush current during power on of the instrument.
The smoothed primary voltage is fed to the chopper FET's Q1 and Q2.
These FET's will cut (with a certain frequency) the primary voltage in parts. The width of these parts (energy contents) is determined by the ***pulse width modulator*** (PWM) IC1 of control circuit 1.
To protect Q1 against high flyback voltage peaks the following protection components are used: D1, C9, R3, C15, D3 and D4. The same protection principle is used for Q2.
Transformer's T4 and T5 are the control transformers through which the square wave control voltages are sent from the PWM to the chopper FET's.
The chopped primary voltage is sent to transformer T1. The secondary coils of this transformer supply the +12V ,+5V and -5V unrectified ac voltages.
In this way the primary mains voltage is separated from the secondary side.
To sense the primary current through transformer T1 a ***current sense transformer*** T3 is connected in series. Its secondary side is connected to the control section of the PWM.

3.2.2.2 The control circuit 1.

This circuit mainly controls the primary circuit with IC1.
IC1 is a switch mode pulse width modulation circuit.
It contains an on chip oscillator, dead time control stage, error amplifier, +5V reference circuit and a push-pull output stage.
Via resistors R21, R22 and VR2, the +5V output voltage of the power supply is compared with the internal reference voltage of IC1.
Pin 1 and 2 of IC1 are inputs of the internal error amplifier to which VR2 and joint R18, R16 are connected.
Pin 14 delivers the reference +5V to R18. Now a voltage of 2.5V will appear on the joint of R18, R16.
The voltage difference between the wiper of VR2 and joint R18, R16 (the error voltage) is amplified by the error amplifier to correct the pulse-width of the output stage, controlling the primary choppers.
In this way a stabilization is realized.
The frequency (±50 kHz) of the output pulses (chopping rate) is determined by R13 and C19.
Pin 3 is used as feedback input for the comparator of the PWM, and pin 4 is connected to a dead time control stage.
When this control stage is activated via transistor Q5 the PWM will switch off.
The push-pull outputs pin 8 and pin 4 of IC1 contain a mutually 180 degrees shifted output block pulse.
These block pulses are sent to Q3 and Q4 to switch the primary coils of driver transformer T4 and T5.

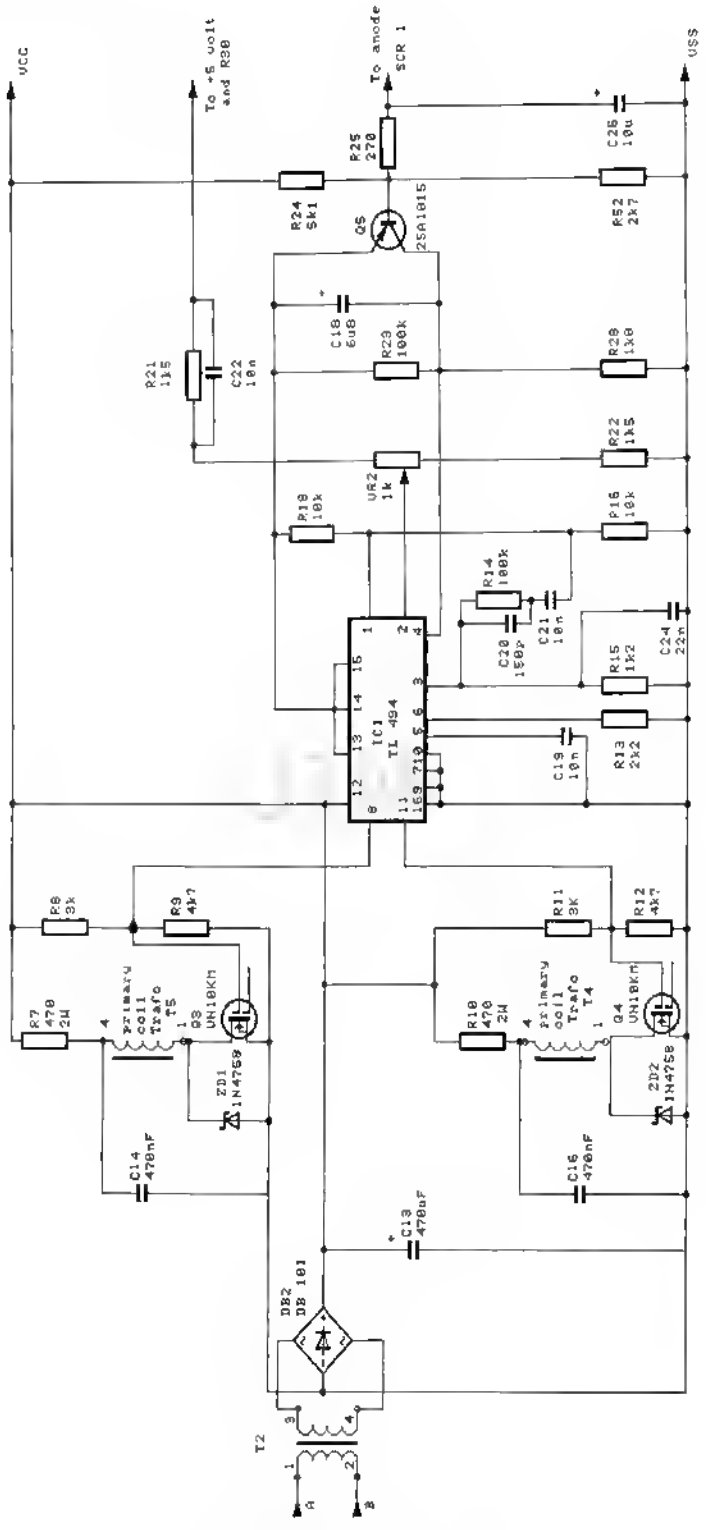


Fig. 3.3. Diagram control circuit 1.

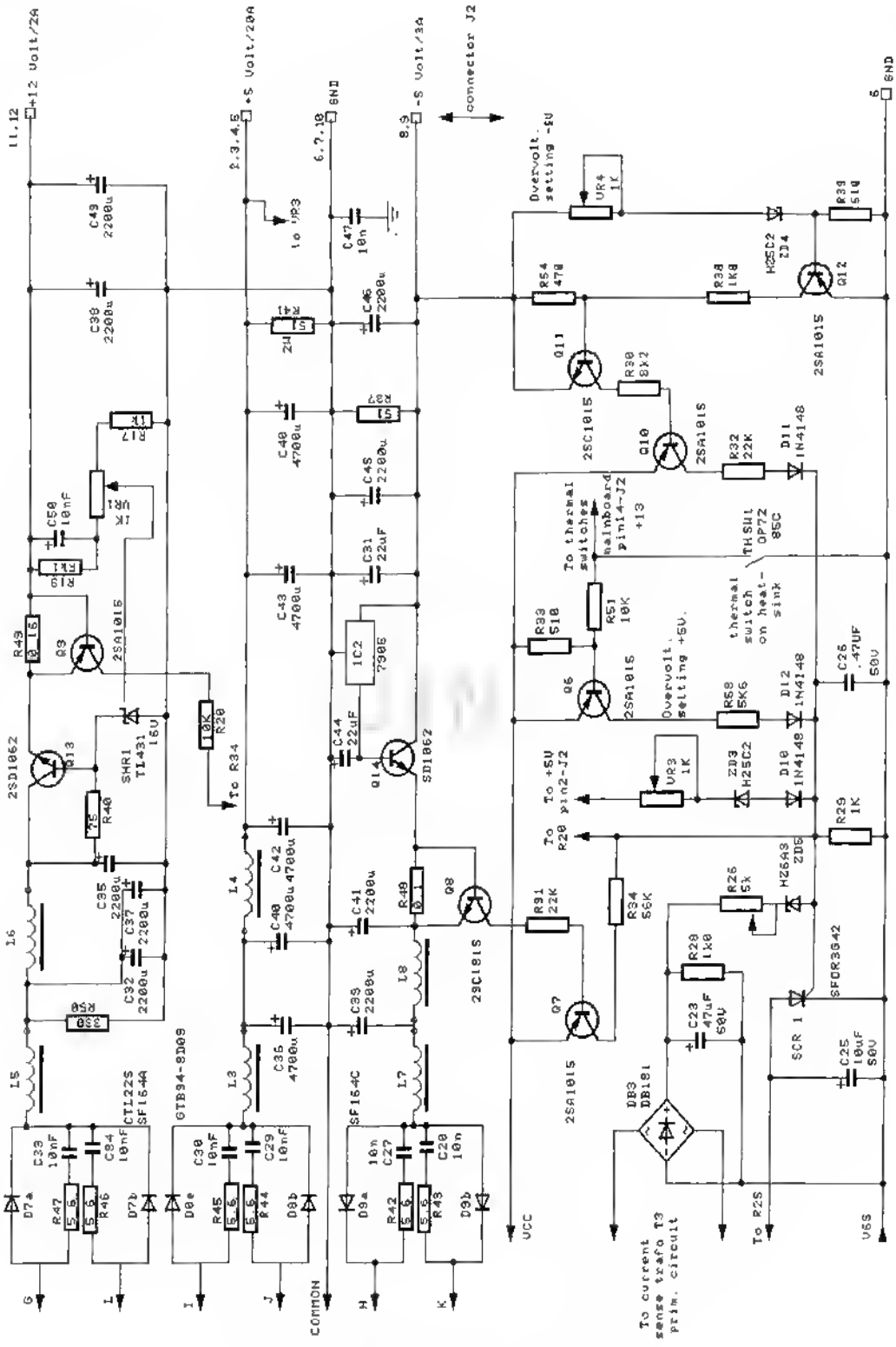


Fig. 3.4. Diagram control circuit 2.

3.2.2.3 The control circuit 2.

This control circuit contains of the secondary stage (current and voltage sensors) and a block of safety protection circuitry.

Secondary stage.

The secondary side of transformer T1 supplies the 3 output voltages for the +12V, +5V and -5V.

- The 12V output.

The output voltage of coil G-L is rectified by diodes D7a and D7b.
A high frequency stop filter is formed by L5, C32, C37, L6 and C35 to block the high frequency chopping transients. By means of potentiometer VR1 the controllable zener diode SHR1 is set to approximately 12.7V. Transistor Q3 will boost this voltage to be a smoothed +12V at 2A rate available at pins 11 and 12 of J2.
An ***over-current sense*** in this output is achieved by resistor R49 and transistor Q9. Via the PWM the power supply is shut down as soon as an over-current situation occurs.

- The +5V output.

The output voltage of coil I-J of T1 is rectified by the diodes D8a and D8b.
Filtering of high frequencies is accomplished by coil L3 and L4. The smoothing of the output voltage is done with a series of capacitors i.e C36, C40, C42, C43 and C45.
There is no serial regulator because of the high current rate of 20A. The stabilization of the output voltage is controlled by the PWM via resistors R21, R22 and the potentiometer VR2.
Over-current in this circuit is sensed by T3 in the primary circuit.

- The -5V output.

The output voltage of coil H-K of T1 is rectified to a negative voltage by diodes D9a and D9b and filtered by L7, C39, L8 and C41.
Stabilizer IC2 will offer an accurate -5V which is boosted by transistor Q14 to a 3A rate.

The safety protection's

The heart of the ***safety protection circuits*** consists of thyristor SCR1.
If this thyristor is activated, the PWM will be shut down, and the power supply switched off.

The +5V and -5V are sensed by safety circuits for over-voltages. Potentiometer VR3 can be aligned in such a way that the thyristor SCR1 is only triggered via ZD3 and D10 if the +5V raises above +5.6V.
Potentiometer VR4 does the same for the -5V output. To obtain a trigger-pulse with a positive polarity for the thyristor, the -5V over-voltage must be inverted. This is obtained via Q10, Q11 and Q12.

To the gate of thyristor SCR1 the primary current sense transformer information is also connected. The higher the primary current, the higher the rectified output voltage of rectifier DB3.
By this there is a linear relation between this rectified voltage and the total secondary current in the power supply. The total power supplied to the secondary circuit before shutdown takes place can be set by R26.

Over-current situations in the +12V are sensed by the thyristor via R49, Q9 and R20 and in the -5V by R48, Q8, R31, Q7 and R34.

An extra protection for excessive temperature is achieved via components Q6, R53 and D12. These components activate the thyristor when either the ***thermal switches*** on the analyzer main-board or the thermal switch on the chopper heatsink shorts R51 to ground.

For alignment of all potentiometers see chapter "Alignments".

3.3 FLOPPY DISK DRIVE.

The ***floppy disk drive*** used is the Epson SMD-340 or SMD-440L super thin 3.5 inch double sided type. Both types are interchangeable and have the same specifications. The only difference is the placement of the flat ribbon cable to the unit. In the SMD-340 this cable is turned 180 degrees compared to the SMD-440L. The cable is key protected in both types.

3.3.1 Drive Performance Specifications.

Single 5V power supply	
Capacity (MFM recording) high density	1474K-bytes
Number of tracks	80 per surface
Maximum recording density	17434 bits/inch
Track density	135 track/inch
Transfer rate	500K-bits/s
Average latency	100ms
Access time (track to track)	3ms
Settling time	15ms
Motor start time	0.5s
Disk rotation speed	300rpm

3.3.2 Drive Reliability.

Mean Time Between Failures	10,000 power on hours
Error rates	
- Soft error rate	1 per 1,000,000,000
- Hard error rate	1 per 1,000,000,000,000
- Seek error rate	1 per 1,000,000

3.3.3 Electronic Circuitry.

A custom made CMOS chip contains all the logic circuitry.
Analog circuitry is also integrated within a single chip operating at +5V.

The main control and read/write circuits are contained on the main-control circuit board. The spindle motor circuit is integrated within the motor control circuit board.

The control circuit consists of:

1. read/write logic and amplifier
2. stepper motor control circuit
3. spindle motor control circuit
4. side select circuit
5. mode select circuit
6. track 00 detection circuit
7. index detection circuit
8. write protect sensor circuit
9. cartridge-in sensor control circuit
10. density detection circuit

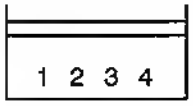
Due to the complexity and high integration rate of the floppy-drive, the unit can only be replaced locally in case of malfunctioning.
There are no field adjustable items or replaceable parts.
The unit must be replaced if faulty.

3.3.3.1 Drive Connectors.

- Power connectors both types.

The small 4-pole power connector is of a key-lock insertion type.
Pin 1 is connected to the +5 volt and pin 2 to ground.
Pin 3 and 4 are not connected.

Layout:

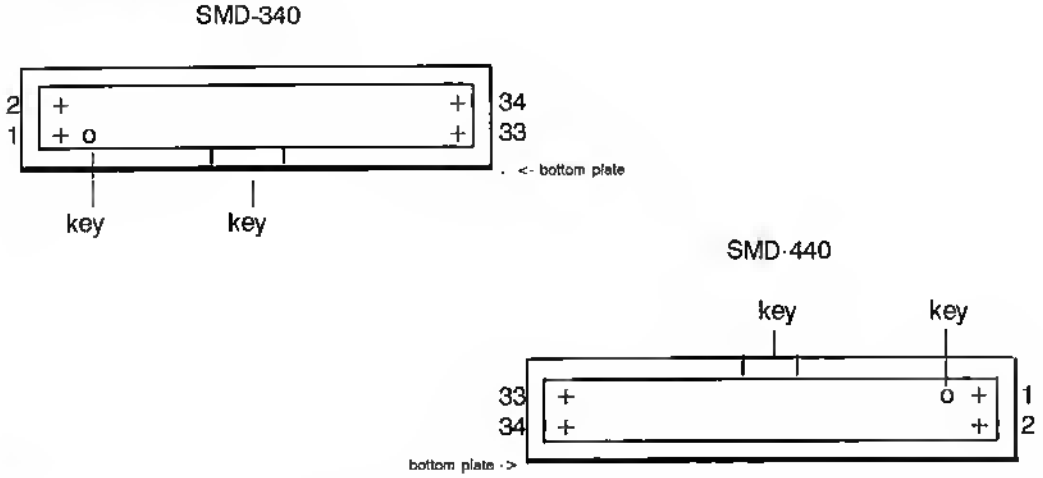


- Signal connector.

The signal connector is a 34 pole type and keyed on the top.
All data and control signals are passed through the flat ribbon cable connected to this connector.
The pin assignment is as follows:

PIN	SIGNAL NAME
1.	N.C.
2.	High Density In (HDI)
3, 4, 5, 6.	N.C.
7, 9, 11.	+5V
8.	Index pulse out (IDX)
10.	Drive select 0 (DS0)
12.	Drive select 1 (DS1)
13,15,17,19,21,23,25,27,29,31,33	Ground
14.	N.C.
16.	Motor On (MON)
18.	Direction (DRTN)
20.	Step (STP)
22.	Write Data (WTD)
24.	Write Gate (WTG)
26.	Track 00 (TK00)
28.	Write Protect (WPT)
30.	Read Data (RDD)
32.	Side Select (SSL)
34.	Disk Change (DCH)

The connector layout:



Care must be taken when the drive is exchanged to ensure that the flat ribbon connector is inserted correctly, according to the key holes, into the frame of the drive.

3.3.4 Setting the jumpers on a replacement floppy drive.

The replacement floppy disk drive should have been received by the customer with the standard settings that are required for use with the PM 3580/PM 3585 logic analyzers. Check for correct ***floppy drive jumpersettings*** before installing the new drive as a replacement unit.

3.3.4.1 SMD-340 Jumper settings.

Fig. 3.5. Location of the jumper block of the SMD-340.

Block	connection	function
A	14 - 15	Drive select 0
B	-	No connections
C	4 - 5	Mode change caused by internal sensors
D	-	Not relevant, not used
E	-	Not relevant, not used

3.3.4.2 SMD-440 Jumper settings

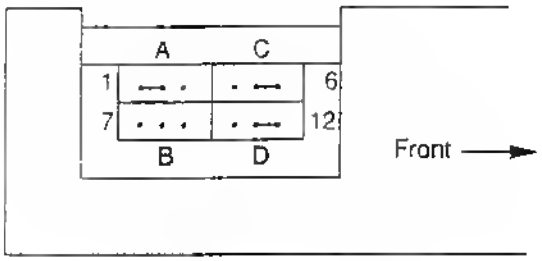


Fig. 3.6. Location of the jumper block of the SMD-440.

Block	connection	function
A Block	1 - 2	Drive select 0
B Block		No connections
C Block	5 - 6	Mode change caused by internal sensors
D Block		Not relevant

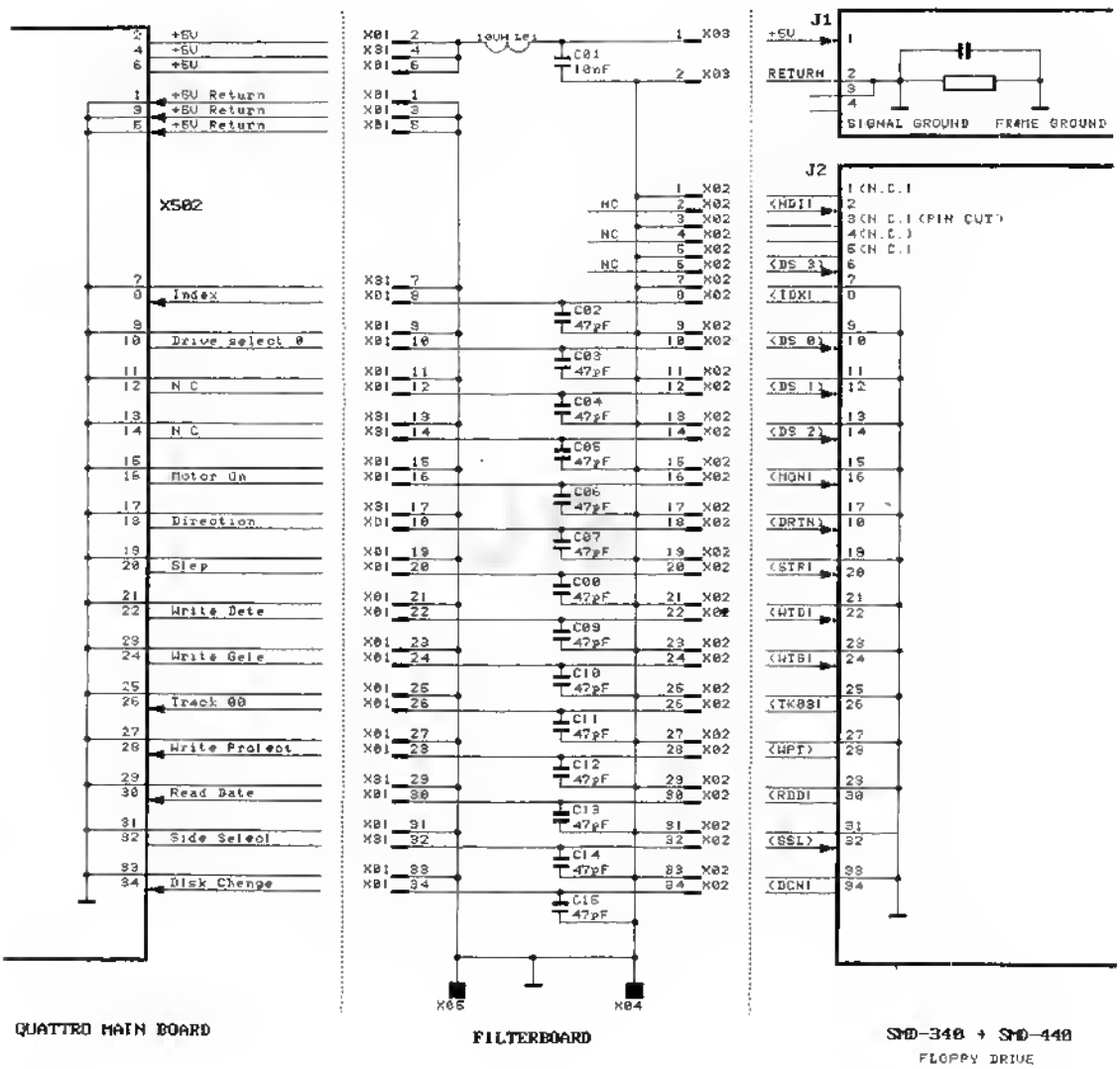


Fig. 3.7. Floppy disk drive interconnections.

3.4 KEYBOARD.

The keyboard is a stand alone unit based on the piggy-back programmed micro-controller 8400 family from PHILIPS.
The micro-controller used is the 84C01 and operates at a 4 MHz speed.
This controller has several 8-bit i/o ports as well as an I^2C communication interface. This communication interface is used to communicate with the analyzers main-board.
The micro-controller is programmed to continuously scan the keys which are mounted in a matrix of horizontal and vertical lines. The horizontal lines are connected to Port 1 and the vertical lines to Port 2.
If a key is depressed a short is made via the key-contact between a certain horizontal line and a vertical line. By decoding which horizontal and which vertical line is involved the micro-controller can identify the key pressed.
By looking up the key-code in the PROM-key-table the correct ASCII code can be found and transmitted to the main-board via the I^2C bus.

The dial key will generate 2 phase-shifted pulses which are analyzed by the micro-controller to determine the direction the dial was moved in. These phase shifted pulses are connected to pin 1 of Port 2 and timer-interrupt input T0 of the micro-controller.

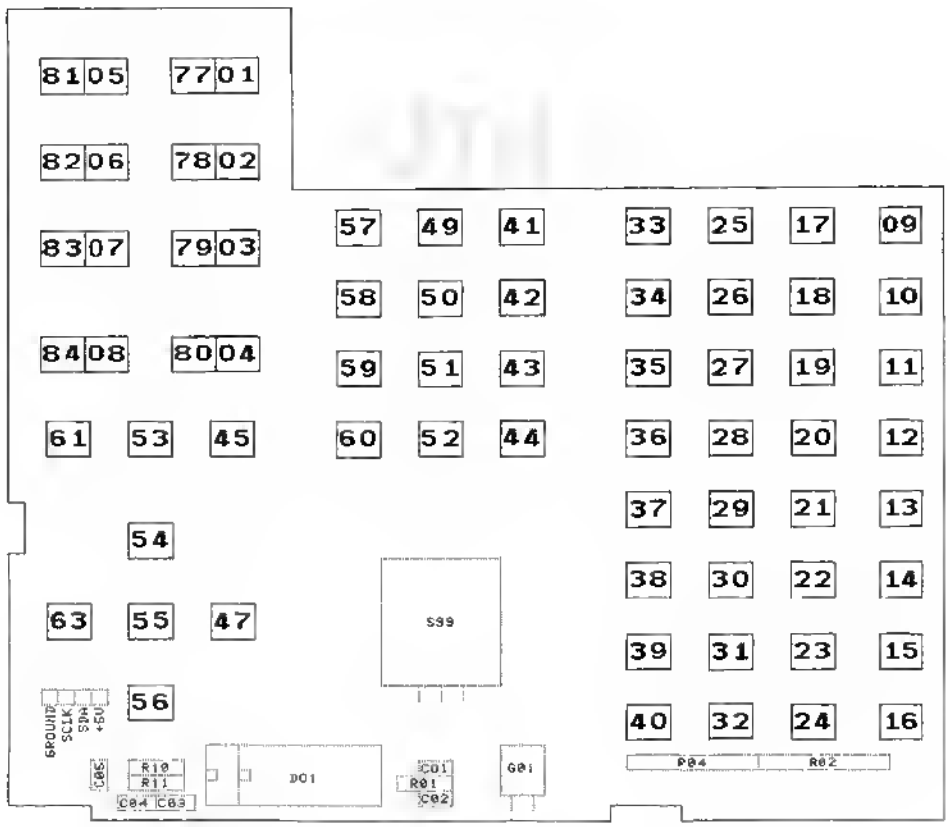


Fig. 3.8. Unit drawing keyboard.

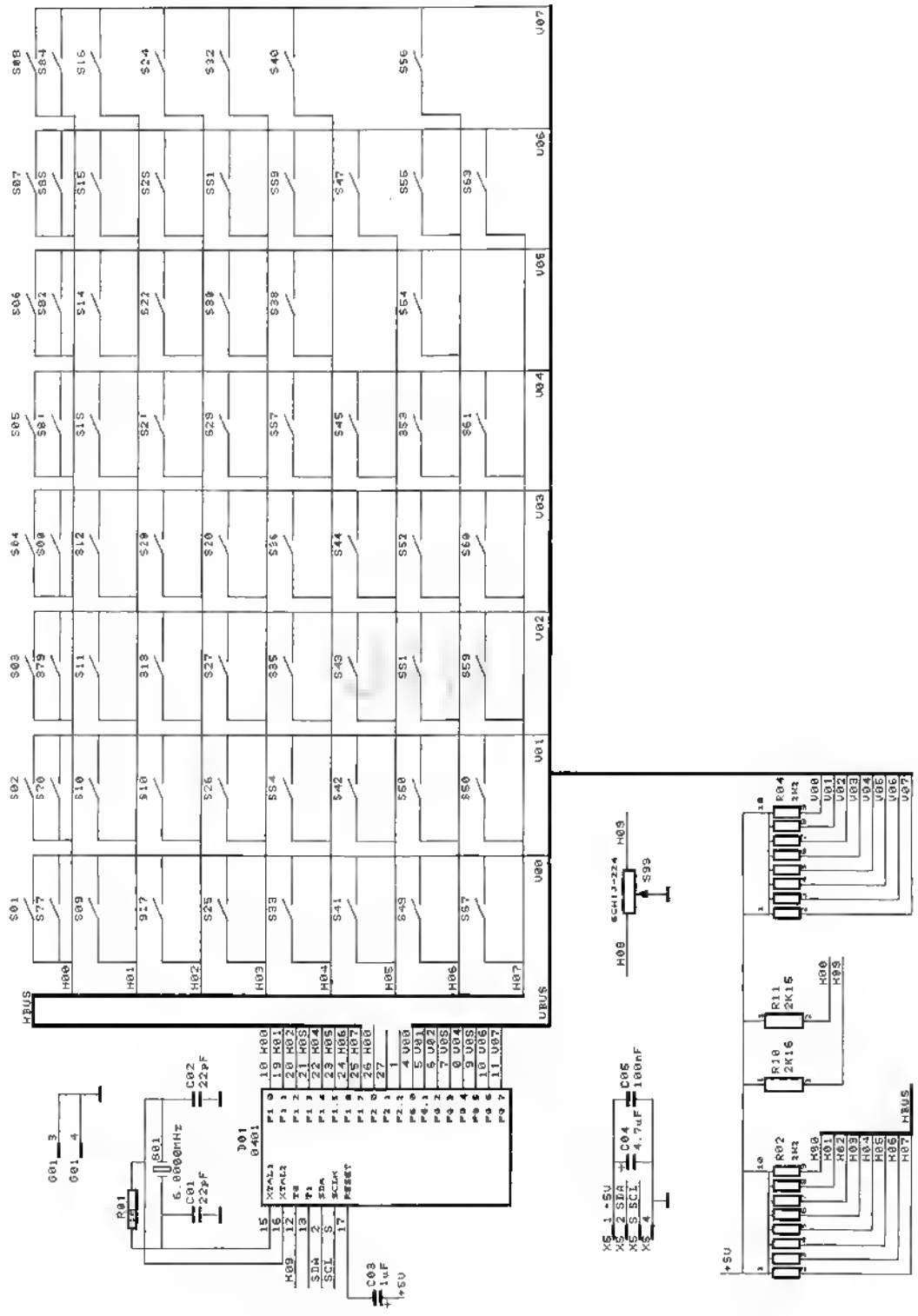


Fig. 3.9. Circuit diagram keyboard.

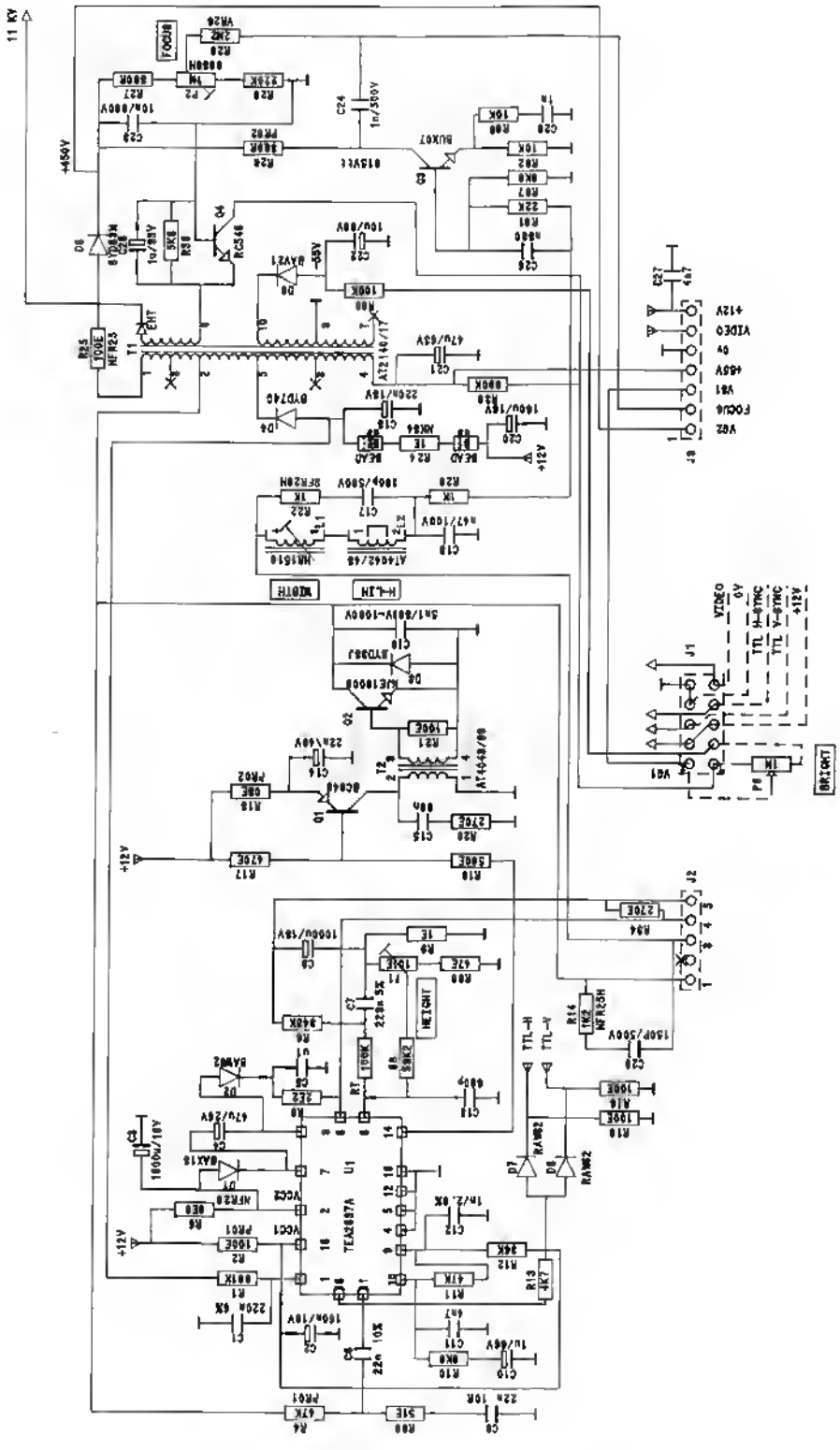


Fig. 3.10. Circuit diagram monitor control board.

3.5 VIDEO MONITOR.

3.5.1 General information.

The video monitor used is composed of a monitor control board attached to the analyzers chassis, a CRT board pressed on the picture tube and the picture tube itself.
The control signals (VSYNC an HSYNC) and power supply (+12V) of the video monitor are all supplied via the 10-pole flat cable coming from the analyzers main-board.

3.5.2 Circuit description.

The control board has three main units i.e.

1. Vertical synchronization and deflection circuit.
2. Horizontal synchronization and deflection circuit.
3. Brightness and E(xtremely) H(igh) T(ension) circuitry.

The items 1 and 2 are all included in I.C. U1 the TEA2037A.
This IC contains:

- 2 free running oscillators (vertical 60 Hz and horizontal 31 kHz)
- a combined sync input followed by sync separator
- a horizontal driver stage
- a vertical output to directly drive the deflection coil

The oscillators are individually triggered by the sync signals coming from the analyzers main-board via connector J1.
Potentiometer P1 sets the vertical deflection amplitude and hence the ***hight of the video picture***.
The horizontal output of U1 is used to drive the line transformer via Q1 and Q2. The line transformer supplies the EHT and focus voltage.
The ***focus of the video picture*** is factory set by potentiometer P2.

The CRT board is connected with a flat ribbon cable to the monitor control board. On the CRT board the video output stage is mounted (transistors Q102 and Q101) as well as some safety bridges for the various picture tube control voltages.

The picture tube's filament is directly heated from the 12V power supply via a resistor of 3.3Ω

On the picture tube the deflection units are mounted as well as a set of ***static deflexion rings*** to align the picture to the centre of the tube.

For all alignments refer to chapter 4 "Adjustments and Jumpersettings"

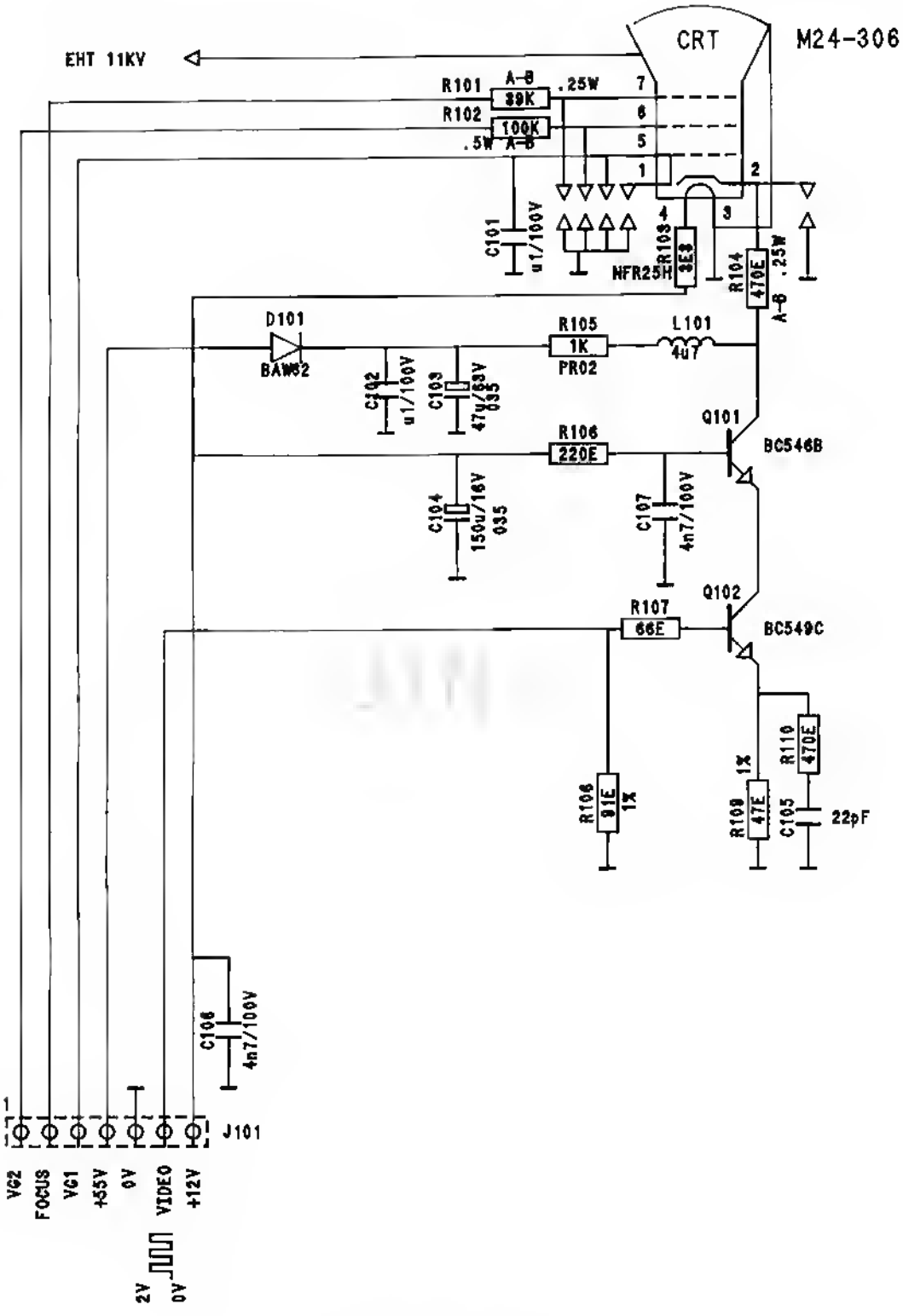


Fig. 3.11. Circuit diagram CRT board.

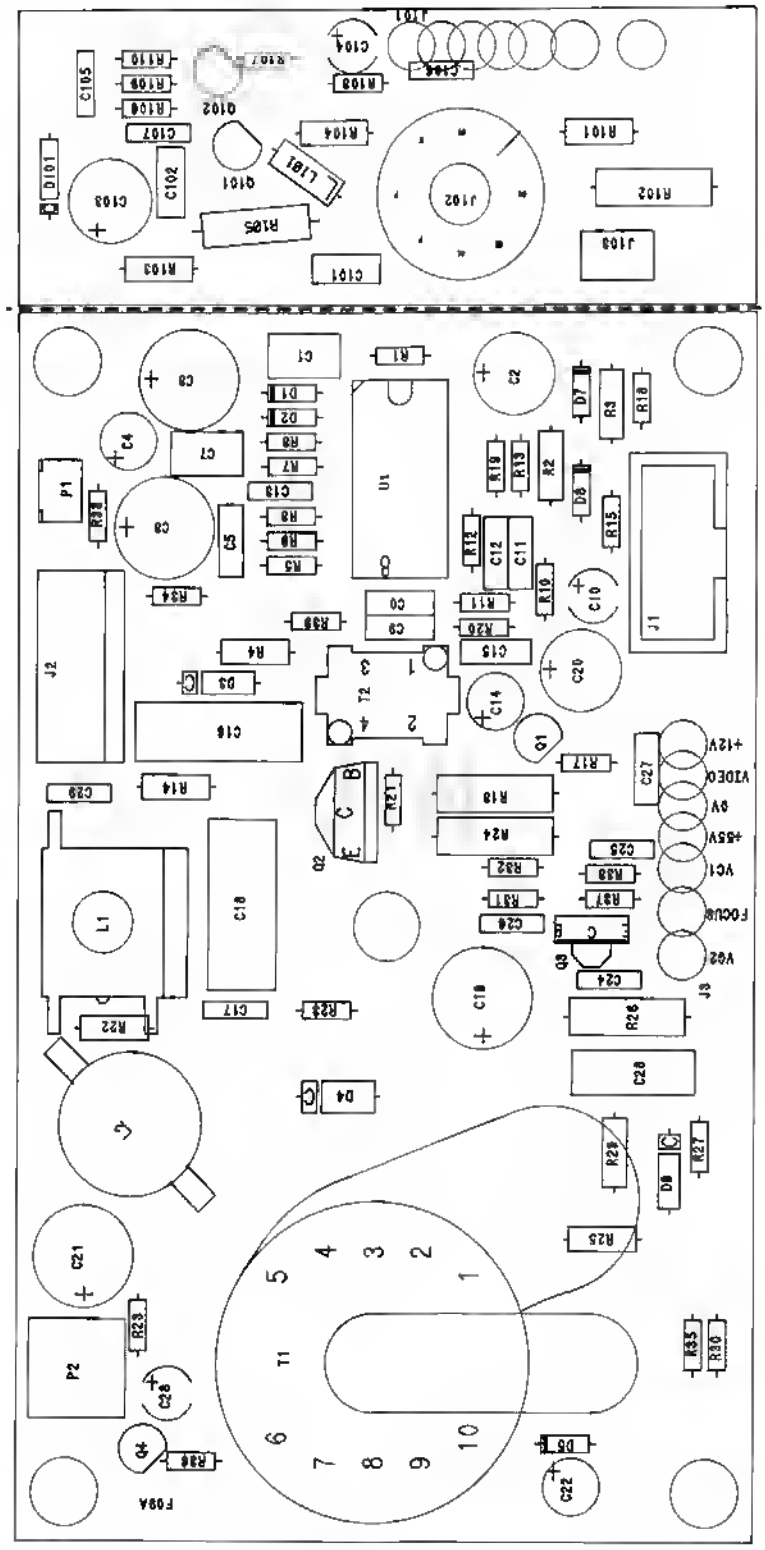


Fig. 3.12. Unit drawing video monitor.

3.6 FAN UNIT.

Electronic circuitry in the fan unit itself is responsible for a stable rotating magnetic field and hence a smooth running of the fan.
The fan unit runs on the +12V from the analyzers main board.

3.7 MAIN-BOARD HARDWARE DESCRIPTION.

3.7.1 General structure main-board.

The following diagram shows the general structure of the analyzer main-board.

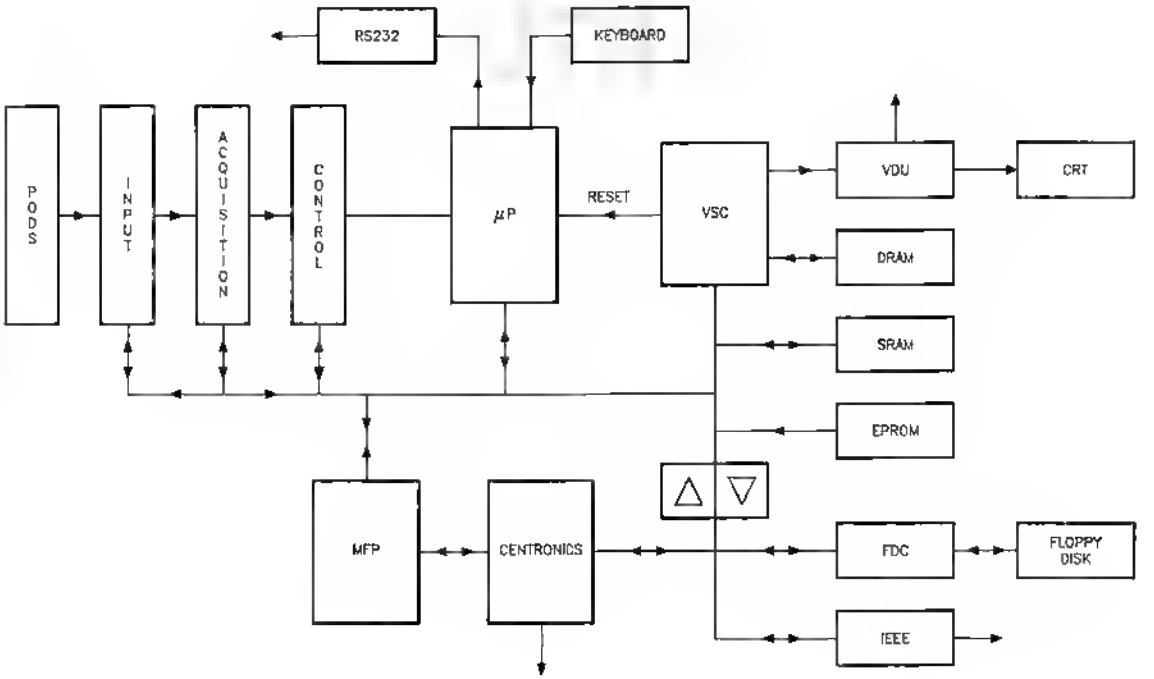


Fig. 3.13. General structure of Analyzer main-board.

3.7.2 The different boards.

There are two different layout's, the 200 MHz board and the 100 MHz board.
The 200 MHz board can be equipped with 96 channels (fully filled) or 64 channels (partly filled board).
The 100 MHz board has a different layout compared with the 200 MHz board and can be equipped with 64 channels (fully filled) or 32 channels (partly filled board).

The chart shows the 4 different boards and their abbreviation names :

200 MHz 96 channels	- 296 board
200 MHz 64 channels	- 264 board
100 MHz 64 channels	- 164 board
100 MHz 32 channels	- 132 board

- The 296 board.

This board is fully equipped to support a 96 channel 200 MHz analyzer.

- The 264 board.

The 200 MHz 64 channel board is a 200 MHz 96 channel board without X5, X6, D5004, D5005, D9, D10, D11, D12 latch D307 and several other small components like resistors and capacitors.
On this board jumpers X5000 and X5001 are present to short the BST chain for the absent Acquisition ASIC's D5004 and D5005.

- The 164 board.

This board is fully equipped to support a 64 channel 100 MHz analyzer.

- The 132 board.

The 100 MHz 32 channel board is a 100 MHz 64 channel board without X3, X4, D5002, D5003, D5, D6, D7, D8 and several other small components like resistors and capacitors.
Also on this board jumpers X5002 and X5003 are present to short the BST chain for the absent Acquisition ASIC's D5002 and D5003.

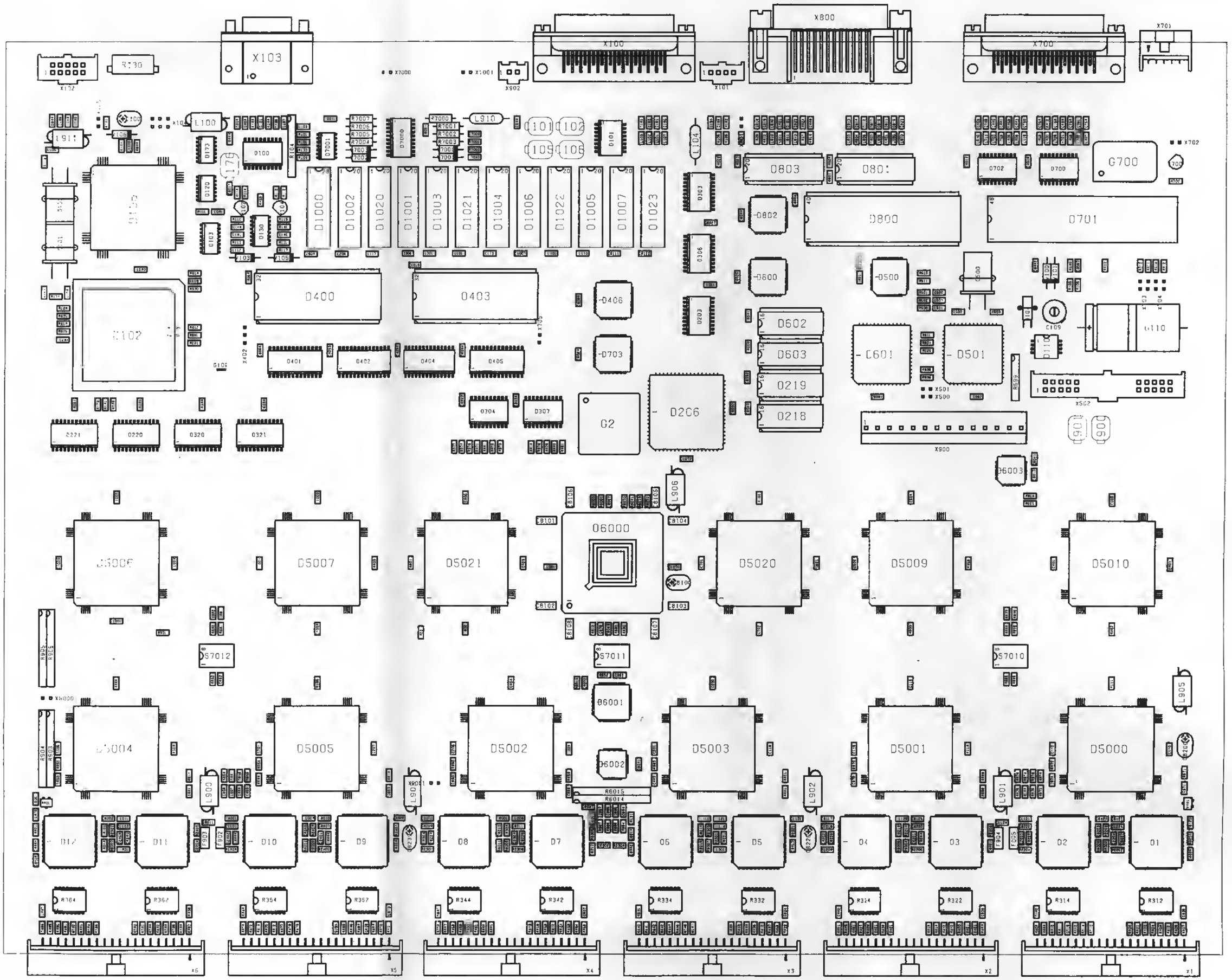
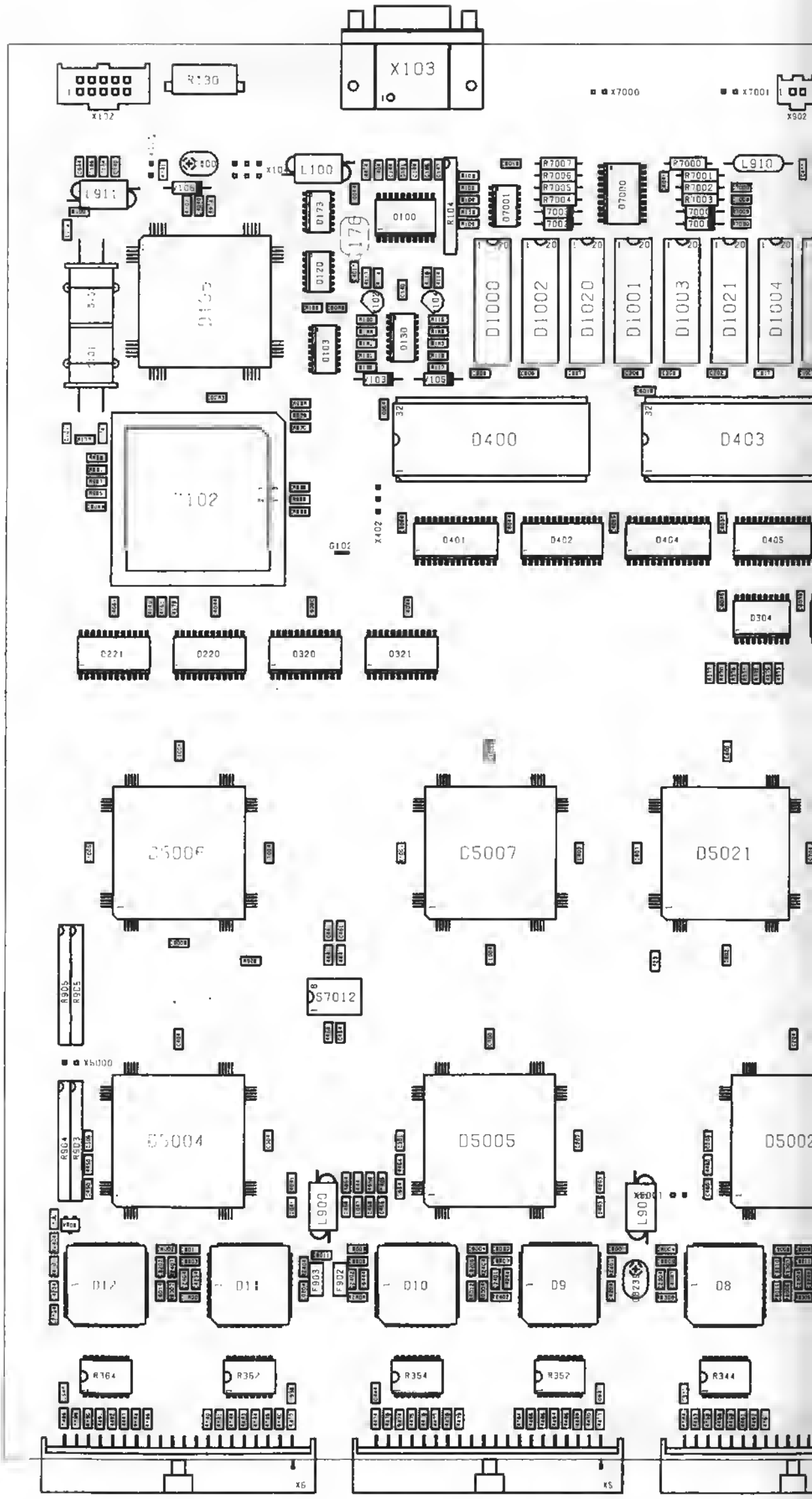


Fig. 3.14. Unit drawing 200 MHz main-board.


X103
R130
X102
X7000
X7001
X902
L100
L910
R104
D100
D1000
D1002
D1020
D1001
D1003
D1021
D1004
D400
D403
D401
D402
D404
D405
D304
D221
D220
D320
D321
D5006
D5007
D5021
S7012
D5004
D5005
L900
L901
D12
D11
D10
D9
D8
R364
R362
R354
R352
R344
X6
X5

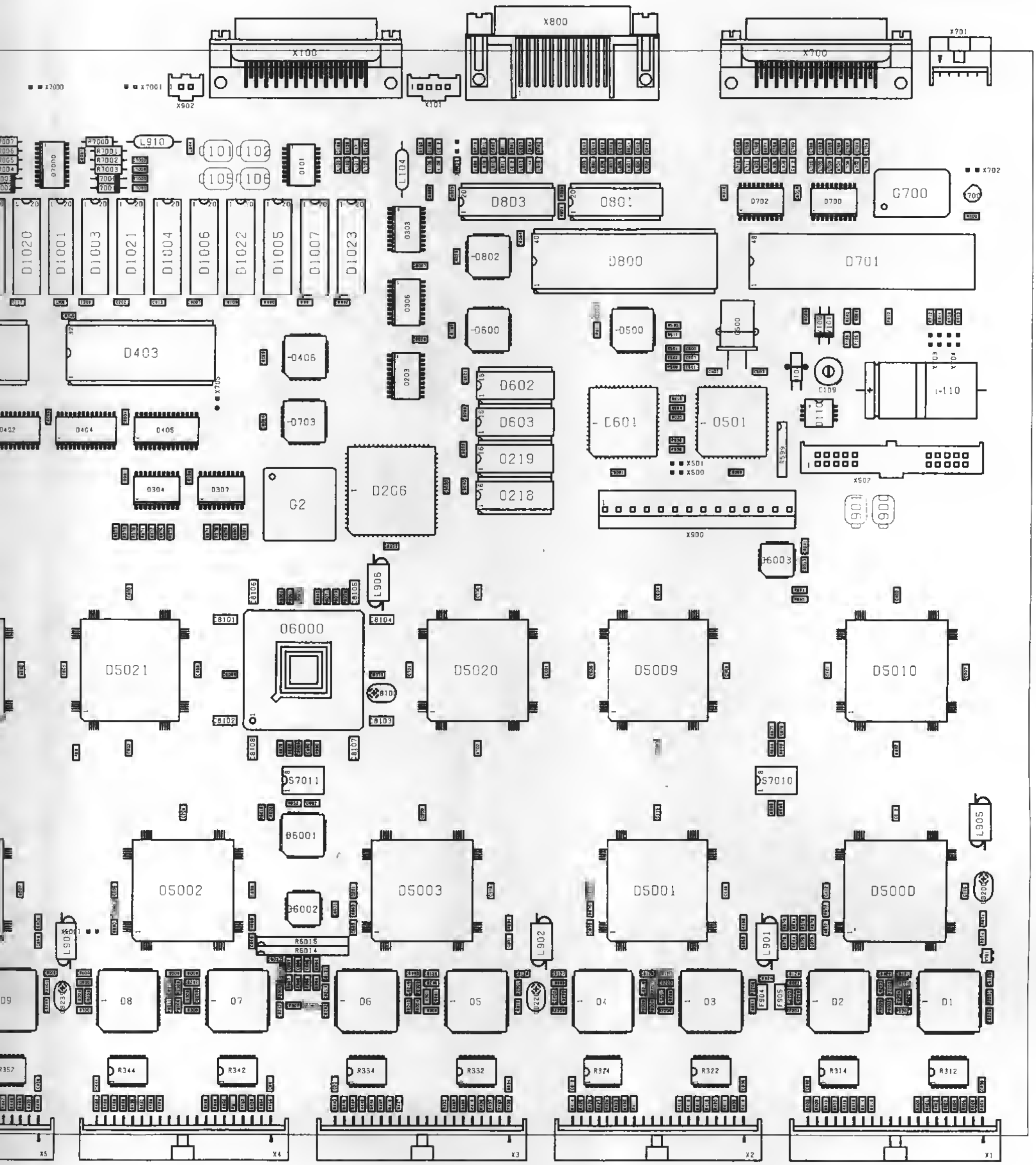


Fig. 3.14. Unit drawing 200 MHz main-board.

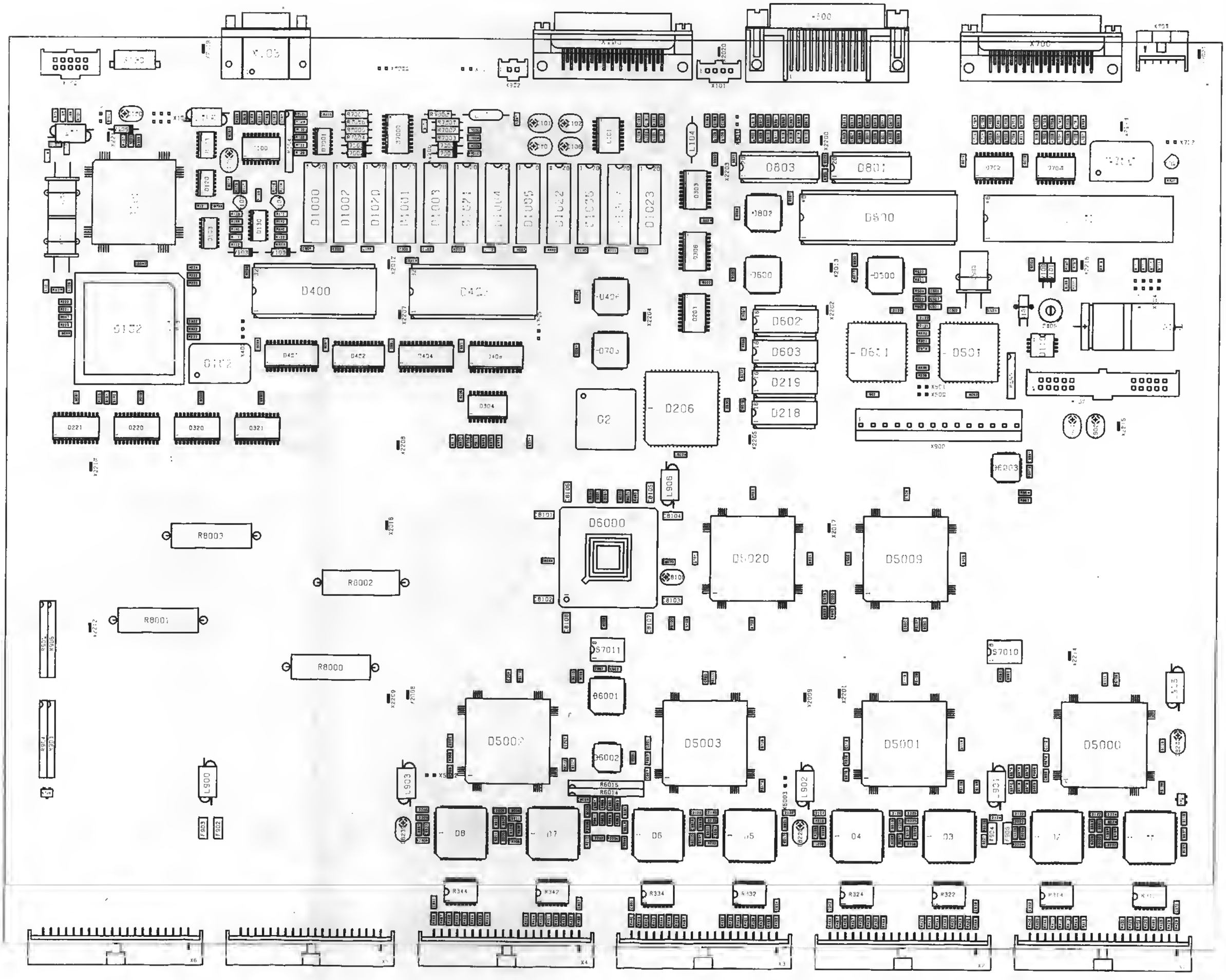
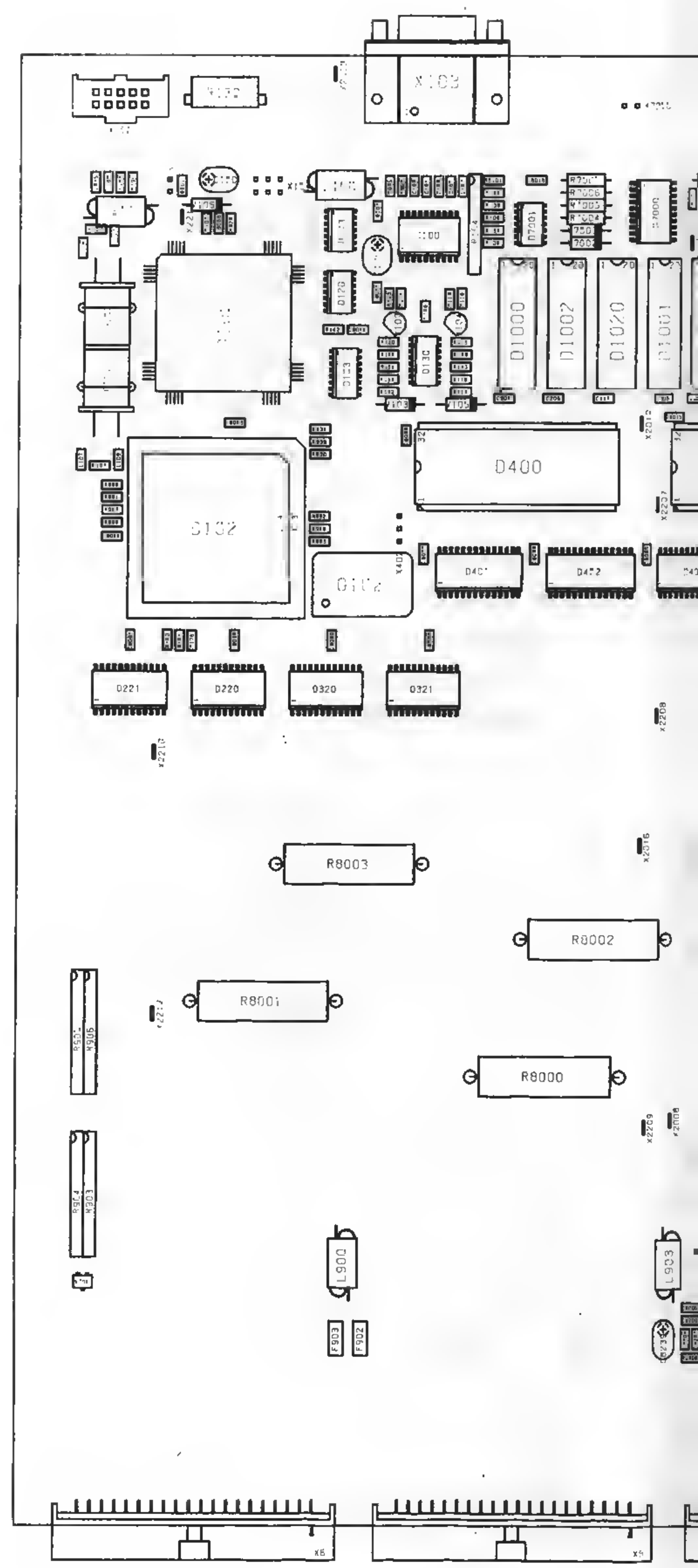


Fig. 3.15. Unit drawing 100 MHz main-board.



X103
D7001
D120
D1000
D1002
D1020
V103
V105
D400
D221
D220
R8003
R8002
R8001
R8000
L900
L903
F903
F902

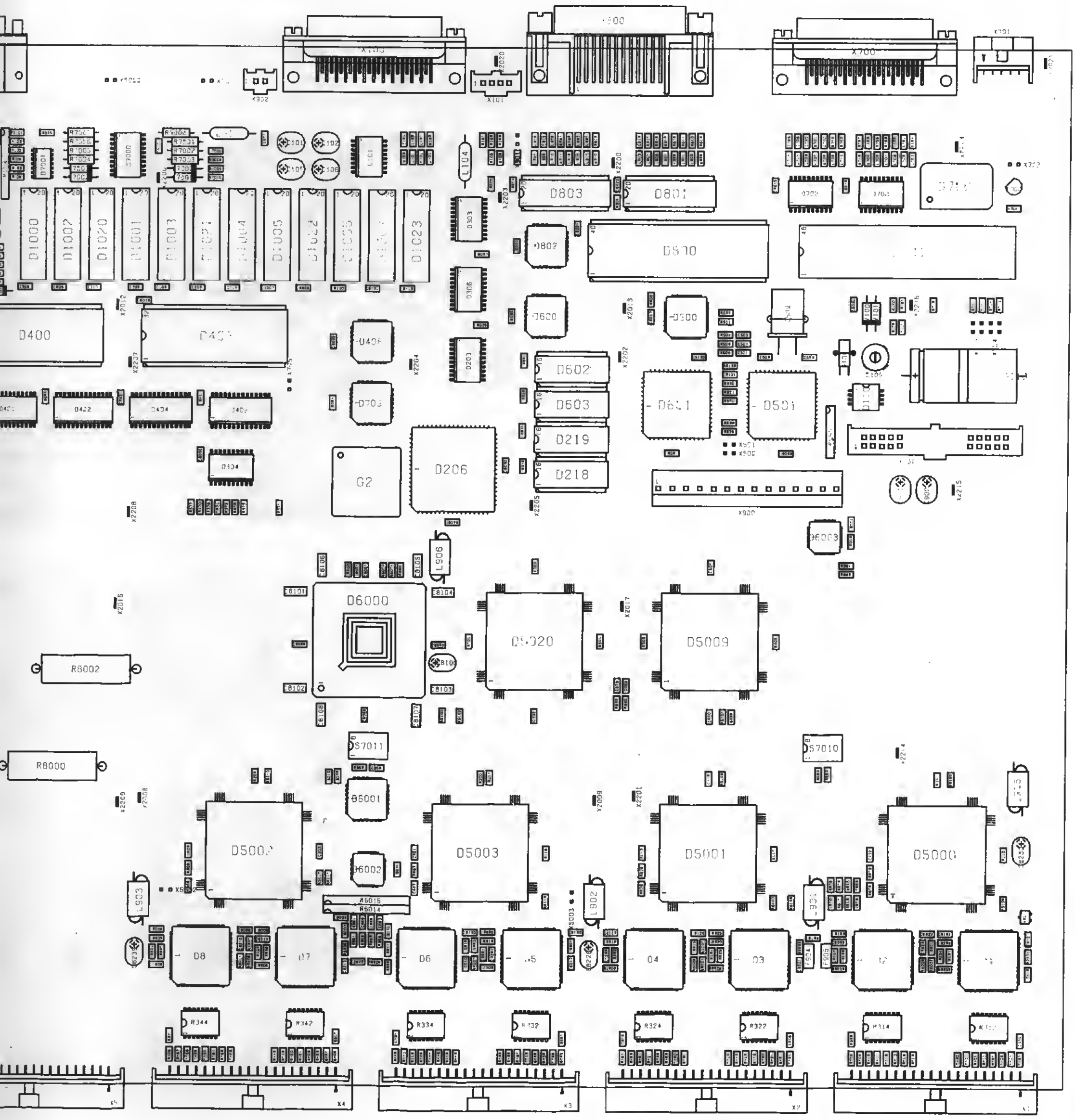


Fig. 3.15. Unit drawing 100 MHz main-board.

3.7.3 The CPU section.

Refer to Fig. 3.16.
The 68070 microprocessor (D102) is a 16 bit processor operating at a 19.6 MHz clock speed. It has on chip DMA control, Memory Management Unit, I^2c bus drive section, built-in timer and a RS232 device.

The 19.6 MHz clock is derived from the xtal G101 and divided by 2 by the CPU to generate 10 MHz bus cycles. The 68070's external bus has 23 non-multiplexed address lines capable of addressing a 16M-byte address range and 16 bit data lines.

There are 7 interrupt levels of which four are decoded interrupts with separate acknowledge outputs IACK2N, 4N, 5N and 7N. Two DMA channels are also available of which only DREQ1N is used for the disk drive.

In order to obtain a proper baud-rate frequency for the RS232 serial output the frequency of G101 is divided by the correct value. G102 is used for baud-rate calculations in future options.

The I^2c bus is used to communicate with the keyboard interface and the real time clock chip. This universal bus is connected to the keyboards 8400 microprocessor which has its own on chip I^2c control device.

The I^2c bus signals are SDA (serial data) and SCL (serial clock).

At Power-On the 68070 is reset by the Video and System Controller SCC66470 (D105). This chip is reset by capacitor C100 or manually via the link X105.

The VSC is a C-MOS 680xx family display and system controller.
It can directly drive up to 2M-bytes of memory and provides chip-select signals for system ROM (D400 and D403). The System ROM is enabled with the signal "CSROM" and the peripherals are enabled with the signal "CSIO".

The on-chip DRAM controller controls 1.5M-byte DRAM (D1000 to D1007 and D1020 to D1023). The CPU can access any memory location even during active video display lines, improving system performance.

The VSC has its own Xtal-frequency of 30 MHz, which is divided by 2 to get the 15 MHz pixel-clock PCLK, and divided by 960 for the 31,25 kHz horizontal synchronisation and divided by 500.000 to get the 60 Hz vertical sync.
The pixel information is clocked by the pixel-clock to the video output VID4-7 on pins 70-73 of the VSC.
These 4 bits comprise 16 grey values on a 15 MHz dot rate. In order to get a 30 MHz dot rate with 4 grey values this 4 bit parallel dot information is clocked with the 30 MHz VCLK through the shift register D103.

The 4 grey values of PIX1 and PIX2 are now demultiplexed by D130 and set to the correct grey value by the attenuator resistor matrix R111, R112, R141 and R144. The video signal is output to the video connector X102 via transistor V102

A corresponding path is used by D100, matrix R116, R117, R142 and R143 and transistor V104 to issue via connector X103 an external video/monitor signal.

After Power-On the VSC is reset and the software will read the 3 CAS inputs (pins 109 to pin 111). Via the pull-up resistors R102, R103 and R133, the CPU can determine how many 512K-byte memory banks are available. The CAS lines are then used as refresh strobe lines for the DRAM's.

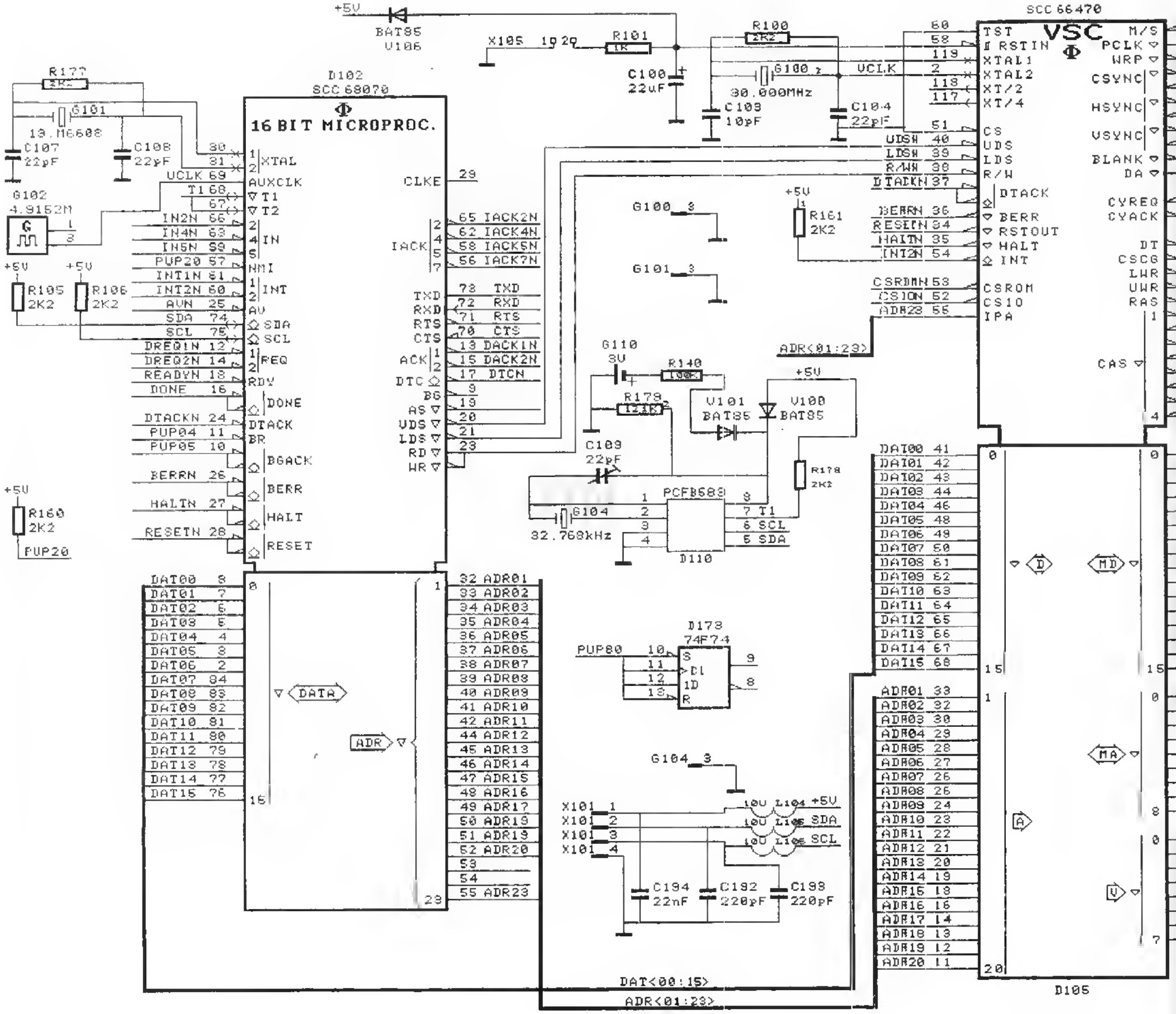
Timer IC D110 (PCF 8583) contains all necessary hardware to keep the time and date correct. The Xtal frequency of 32.78677 kHz is divided by 2^{15} to interrupt every second the 68070 processor via pin 17. (T1 of D110).
Via the I^2c bus the time is sent to the microprocessor.
All the internal RAM, as-well the oscillator circuit of the timer IC, are powered by battery G110 during power off of the analyzer.

3.7.3.1 The RS232 port.

The RS232 port of the CPU is connected to the outside world (X100) by one chip only, the MAX 232 (D101).

This chip generates its own RS232 voltages (-9V and +9V) for line communication via the lines Transmit (TX), Receive (RX), Request To Send (RTS) and Clear To Send (CTS).

Fig. 3.16. The CPU section.


+5V
BAT85
V106
X105
R101
1K
R100
2K2
C100
22uF
G100
30.000MHz
C103
10pF
C104
22pF
VCLK
SCC 66470
VSC
TST
RSTIN
XTAL1
XTAL2
XT/2
XT/4
CS
UDS
LDS
R/W
DTACKN
DTACK
BERR
RSTOUT
HALT
INT
CSRDMN
CSION
ADR23
CSROM
CS10
IPA
M/S
PCLK
WRP
CSYNC
HSYNC
VSYNC
BLANK
DA
CVREQ
CVACK
DT
CSCG
LWR
UWR
RAS
CAS
R177
2K2
G101
13.M6608
C107
22pF
C108
22pF
G102
4.9152M
UCLK 69
T1 68
IN2N 66
IN4N 63
IN5N 59
PUP20 57
INT1N 61
INT2N 60
AVN 25
SDA 74
SCL 75
DREQ1N 12
DREQ2N 14
READYN 18
DONE 16
DTACKN 24
PUP04 11
PUP05 10
BERRN 26
HALTN 27
RESETN 28
R105
2K2
R106
2K2
R160
2K2
PUP20
D102
SCC 68070
16 BIT MICROPROC.
XTAL
AUXCLK
T1
T2
IN
NMI
INT
AV
SDA
SCL
REQ
RDY
DONE
DTACK
BR
BGACK
BERR
HALT
RESET
CLKE
IACK2N
IACK4N
IACK5N
IACK7N
TXD
RXD
RTS
CTS
DACK1N
DACK2N
DTCN
BG
AS
UDS
LDS
RD
WR
G110
3V
R140
R179
121K
V101
BAT85
V100
BAT85
C109
22pF
G104
32.768kHz
PCF8583
D110
R178
2K2
G100
G101
R161
2K2
ADR<01:23>
D173
74F74
PUP80
DATA
ADR
DAT00 8
DAT01 7
DAT02 6
DAT03 5
DAT04 4
DAT05 3
DAT06 2
DAT07 84
DAT08 83
DAT09 82
DAT10 81
DAT11 80
DAT12 79
DAT13 78
DAT14 77
DAT15 76
ADR01 32
ADR02 33
ADR03 34
ADR04 35
ADR05 36
ADR06 37
ADR07 38
ADR08 39
ADR09 40
ADR10 41
ADR11 42
ADR12 44
ADR13 45
ADR14 46
ADR15 47
ADR16 48
ADR17 49
ADR18 50
ADR19 51
ADR20 52
ADR23 55
G104
X101
L104
L105
L106
SDA
SCL
C194
22nF
C192
220pF
C198
220pF
DAT<00:15>
ADR<01:23>
DAT00 41
DAT01 42
DAT02 43
DAT03 44
DAT04 46
DAT05 48
DAT06 49
DAT07 50
DAT08 61
DAT09 62
DAT10 63
DAT11 64
DAT12 65
DAT13 66
DAT14 67
DAT15 68
ADR01 33
ADR02 32
ADR03 30
ADR04 29
ADR05 28
ADR06 27
ADR07 26
ADR08 26
ADR09 24
ADR10 23
ADR11 22
ADR12 21
ADR13 20
ADR14 19
ADR15 18
ADR16 16
ADR17 14
ADR18 13
ADR19 12
ADR20 11
D
MD
MA
A
V
D105

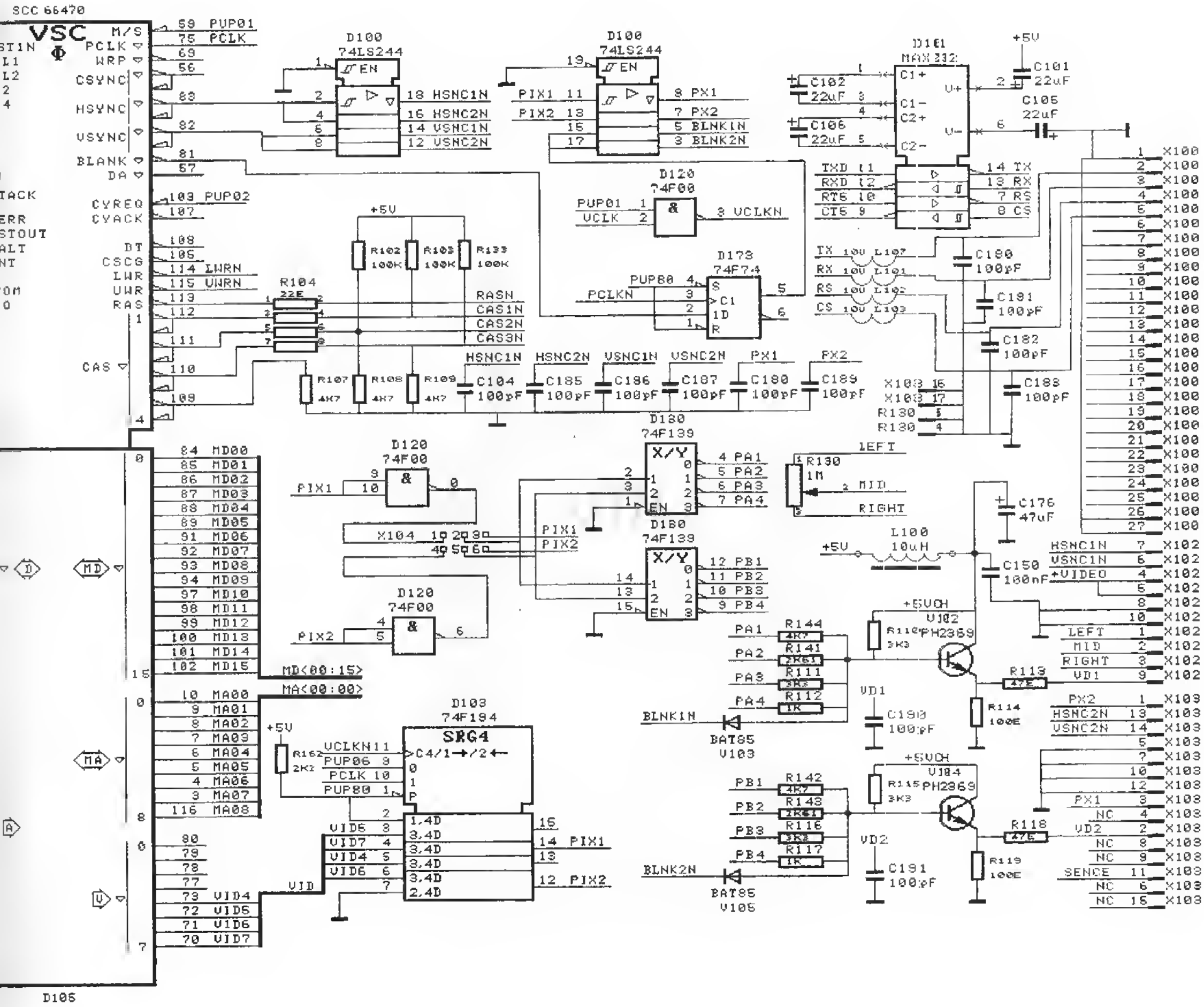


Fig. 3.16. The CPU section.

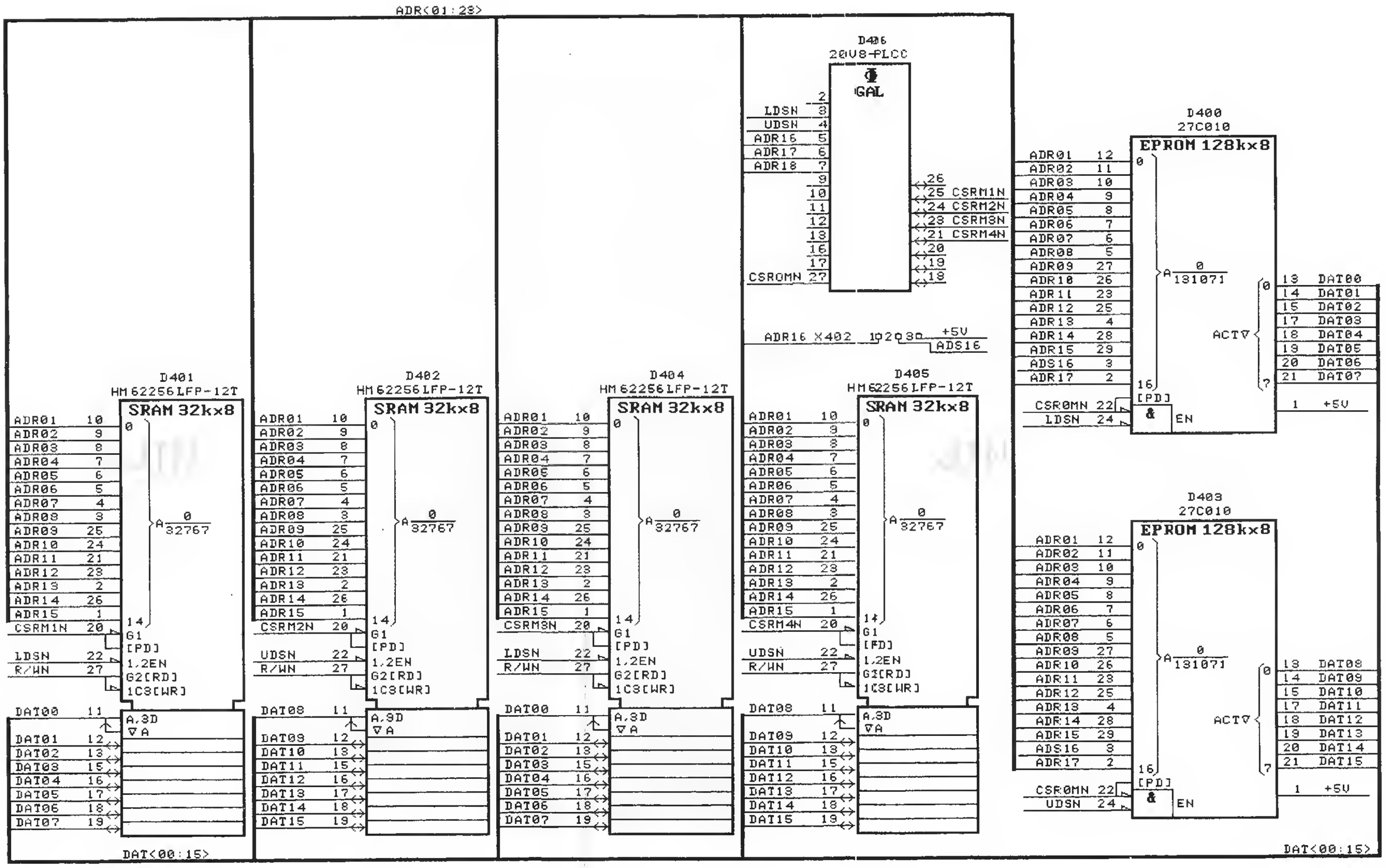
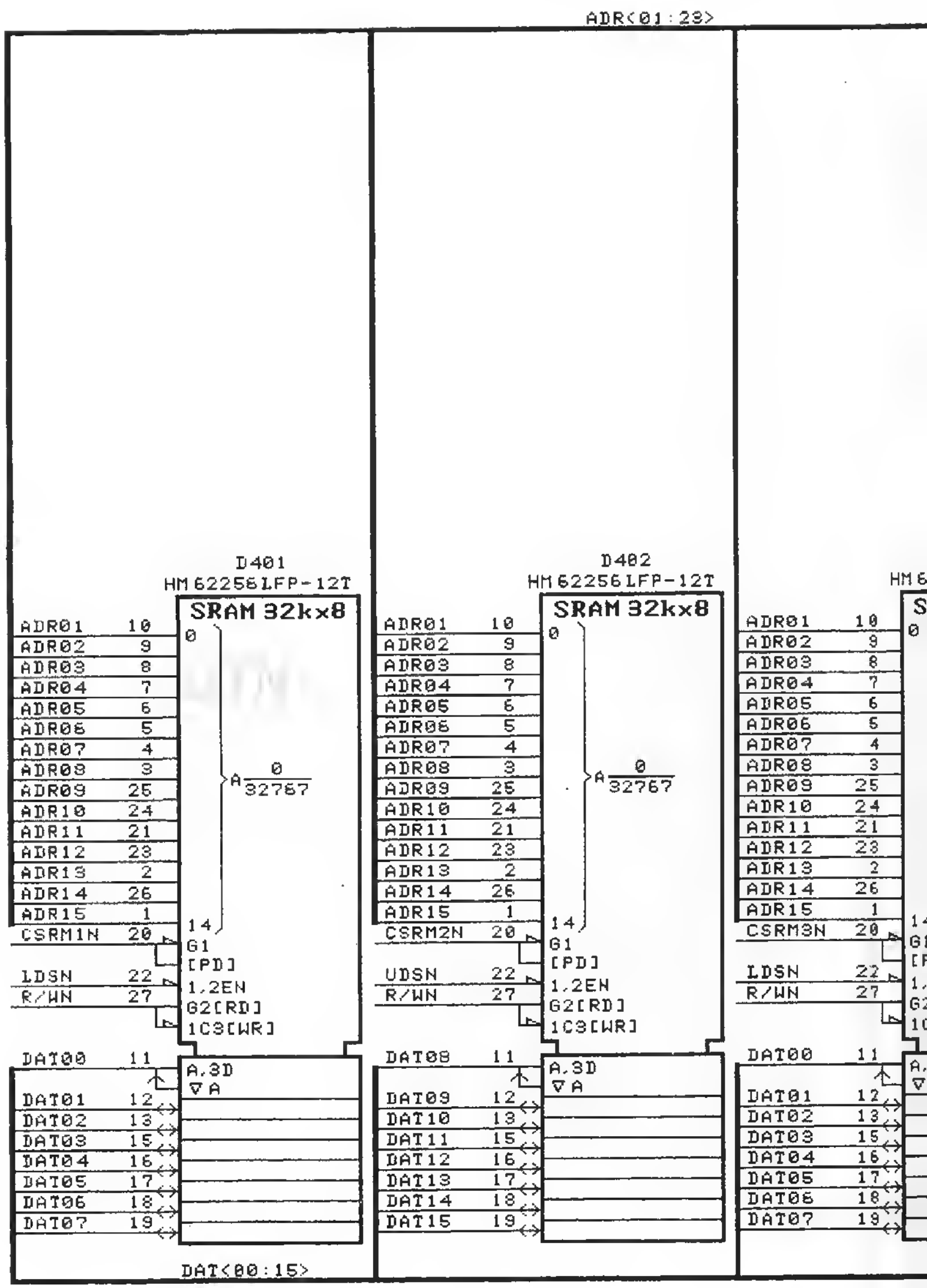


Fig. 3.17. The Static RAM and EPROM.


ADR<01:23>
D401
HM62256LFP-12T
SRAM 32kx8
ADR01 10
ADR02 9
ADR03 8
ADR04 7
ADR05 6
ADR06 5
ADR07 4
ADR08 3
ADR09 25
ADR10 24
ADR11 21
ADR12 23
ADR13 2
ADR14 26
ADR15 1
CSRM1N 20
LDSN 22
R/WN 27
DAT00 11
DAT01 12
DAT02 13
DAT03 15
DAT04 16
DAT05 17
DAT06 18
DAT07 19
0
14
A 0 32767
G1
[PD]
1,2EN
G2[RD]
1C3[WR]
A,3D
▽A
D402
HM62256LFP-12T
SRAM 32kx8
ADR01 10
ADR02 9
ADR03 8
ADR04 7
ADR05 6
ADR06 5
ADR07 4
ADR08 3
ADR09 25
ADR10 24
ADR11 21
ADR12 23
ADR13 2
ADR14 26
ADR15 1
CSRM2N 20
UDSN 22
R/WN 27
DAT08 11
DAT09 12
DAT10 13
DAT11 15
DAT12 16
DAT13 17
DAT14 18
DAT15 19
0
14
A 0 32767
G1
[PD]
1,2EN
G2[RD]
1C3[WR]
A,3D
▽A
ADR01 10
ADR02 9
ADR03 8
ADR04 7
ADR05 6
ADR06 5
ADR07 4
ADR08 3
ADR09 25
ADR10 24
ADR11 21
ADR12 23
ADR13 2
ADR14 26
ADR15 1
CSRM3N 20
LDSN 22
R/WN 27
DAT00 11
DAT01 12
DAT02 13
DAT03 15
DAT04 16
DAT05 17
DAT06 18
DAT07 19
DAT<00:15>

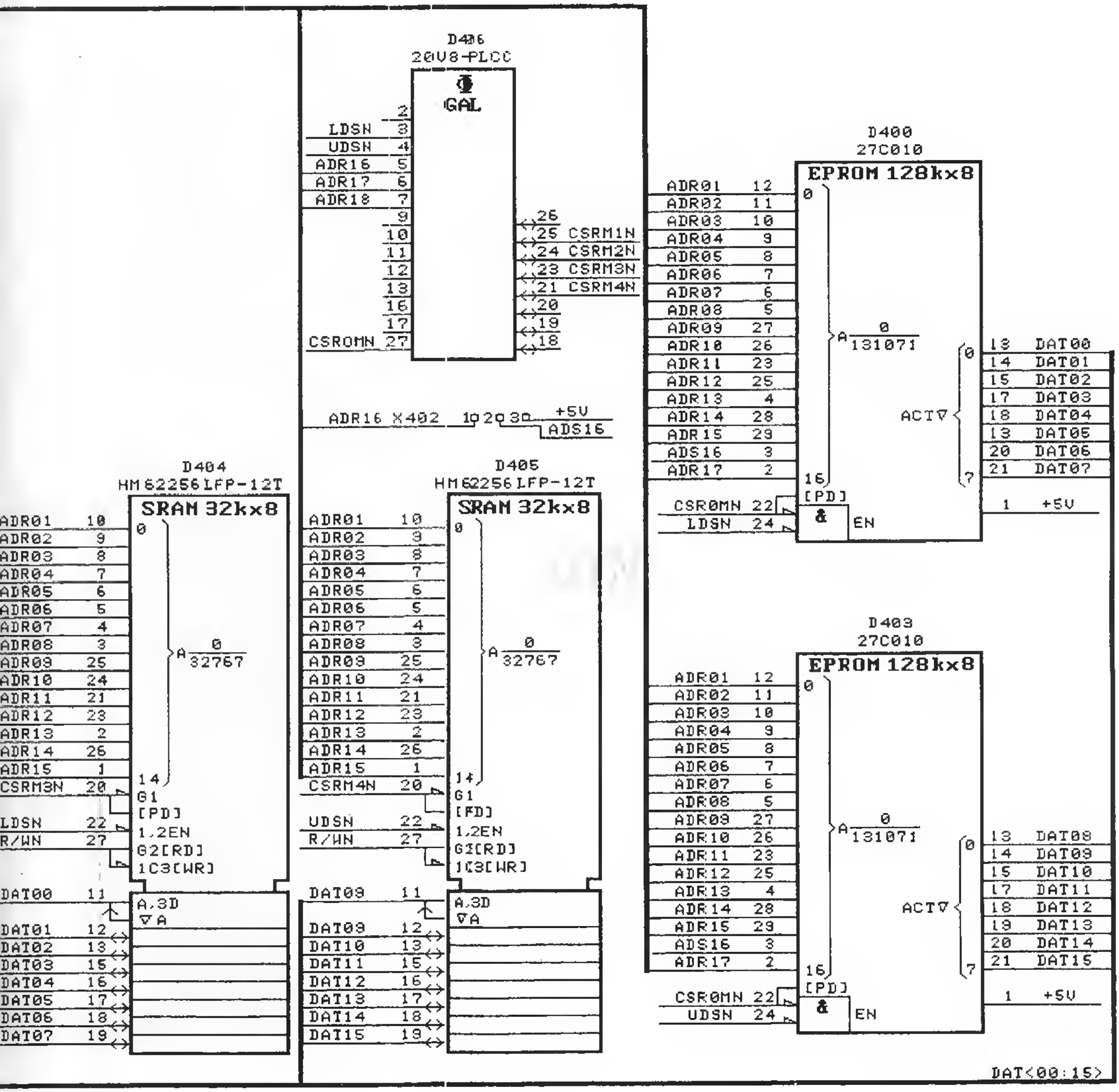


Fig. 3.17. The Static RAM and EPROM.

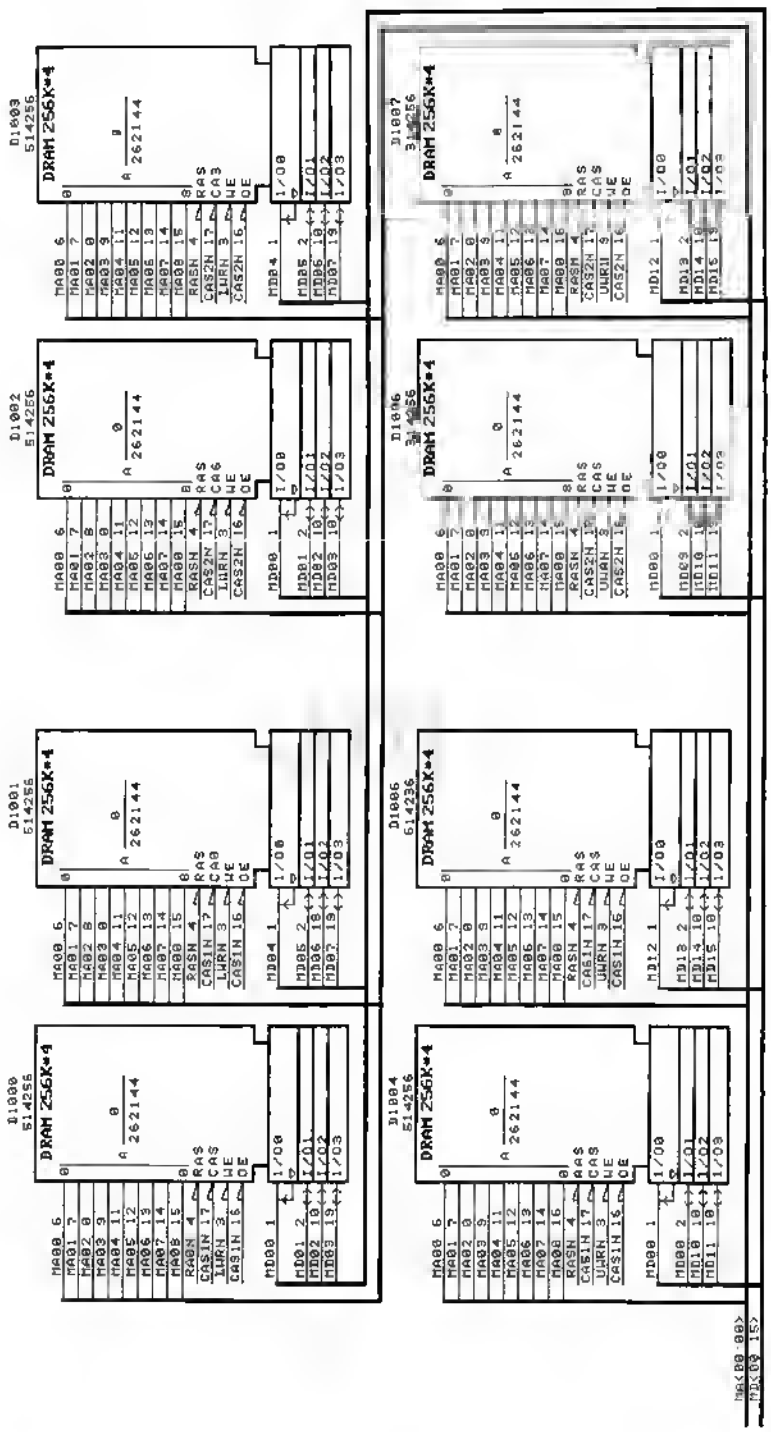


Fig. 3.18. The Dynamic RAM (part 1).

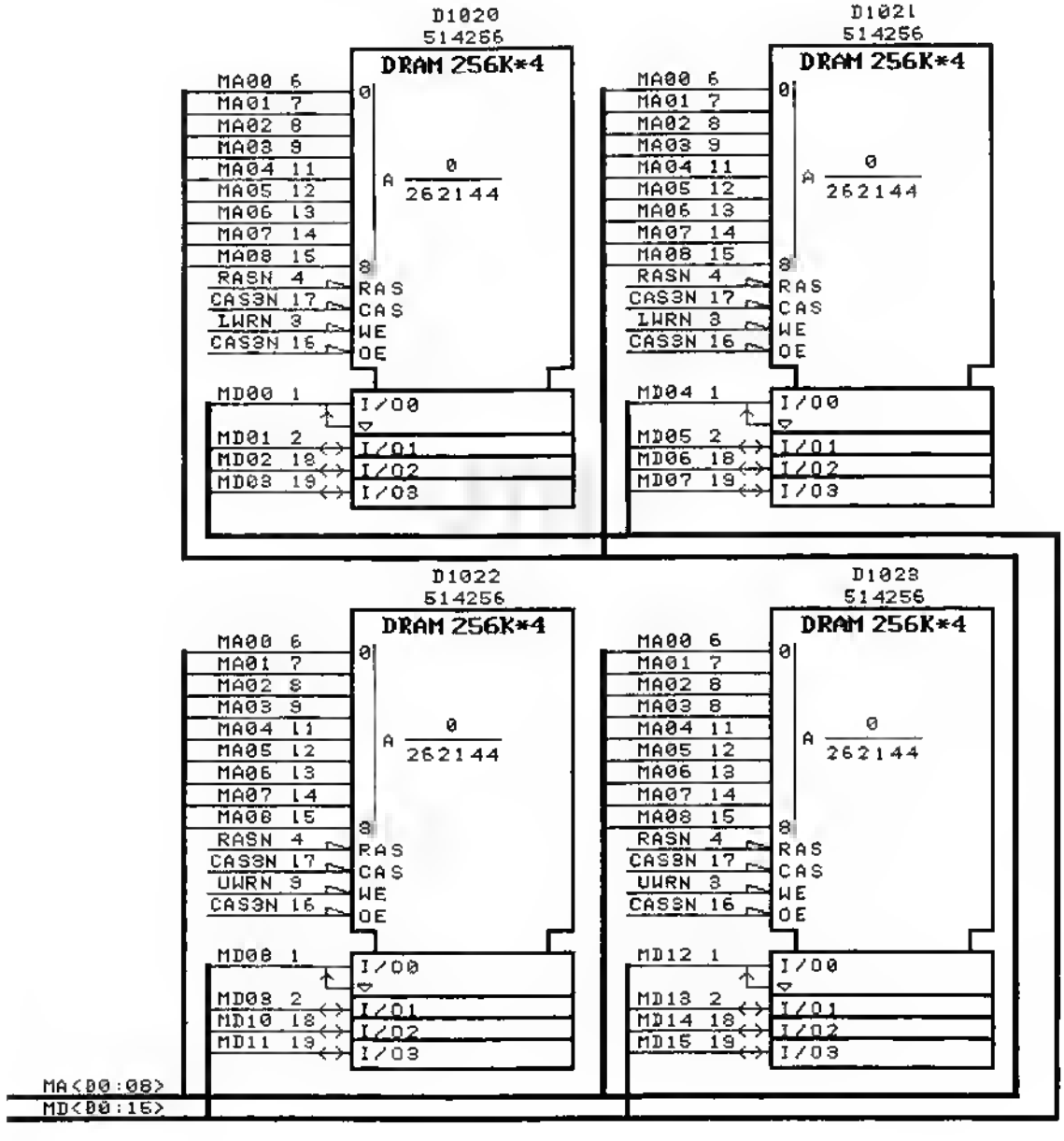


Fig. 3.19. The Dynamic RAM (part 2).

3.7.3.2 The Static RAM.

Refer to Fig. 3.17.
The SRAM's are of the HM 62256LFP-12T type and are 32K-byte x 8 = 256K-bit wide.
In total there are 2 banks. Bank1 (D401 and D402) and Bank2 (D404 and D405).
Each bank has an odd and an even byte selected by the GAL (Generic Array Logic) address decoding IC D406. Depending on the CPU access, words or bytes are selected.

3.7.3.3 The EPROM's.

Refer to Fig. 3.17.
The resident analyzer software is stored in the 2 EPROM's. These can be any of the following three types; 27256, 27512 or 27010. Depending on the type used, address line ADS16 must be activated and strap X402 must be set accordingly. These settings are:

27256 2-3 connected*
27512 1-2 connected*
27010 1-2 connected

* These types must be positioned to the right-hand side of the socket (towards the battery backup).

The EPROM chip select is derived from a GAL (D703).

3.7.3.4 The Dynamic RAM's.

Refer to Fig. 3.18 and 3.19.
The 3 banks of dynamic RAM's are composed of 4 chips per bank. The RAM chip used is the 514256 (256K x 4 Bits). A RAM can store the high or low nibble in a high or low byte of a word.

UDS and LDS strobes sent from the CPU to the VSC are decoded to UWR (Upper Write Read) for the upper RAM bank and LWR (Lower Write Read) for the lower RAM bank.
The RAS and CAS signals are timing refresh signals to keep the memory contents refreshed.

3.7.3.5 Data buffers.

Refer to Fig. 3.20.
There are 2 data buffers (D303 and D306) to communicate with the peripherals and 4 buffers (D304, D307, D321 and D326) for communication with the analyzer part of the main board.
D303 and D306 are both enabled by GAL D802. D303 controls the lower byte of the data bus, while D306 controls the upper byte.
Buffer D304 and D307 are directly connected per bit to an individual Input ASIC (D1 to D12). Also D320 and D321 are directly connected to ASIC's on the analyzer part. These buffers are also prepared to enable the usage of boundary scan tests.

3.7.3.6 Address bus buffers.

Refer to Fig. 3.21.
The CPU address bus ADR01 - ADR11 is buffered for the analyzer part by boundary scan buffers D220 and D221.
The peripheral devices are controlled via ADR01 - ADR05 with buffer D203. The peripheral addresses are named PAD01 - PAD05. On the CPU address bus also D206 is connected, where this ASIC is mainly used for boundary scan and chip select purposes for the analyzer part.

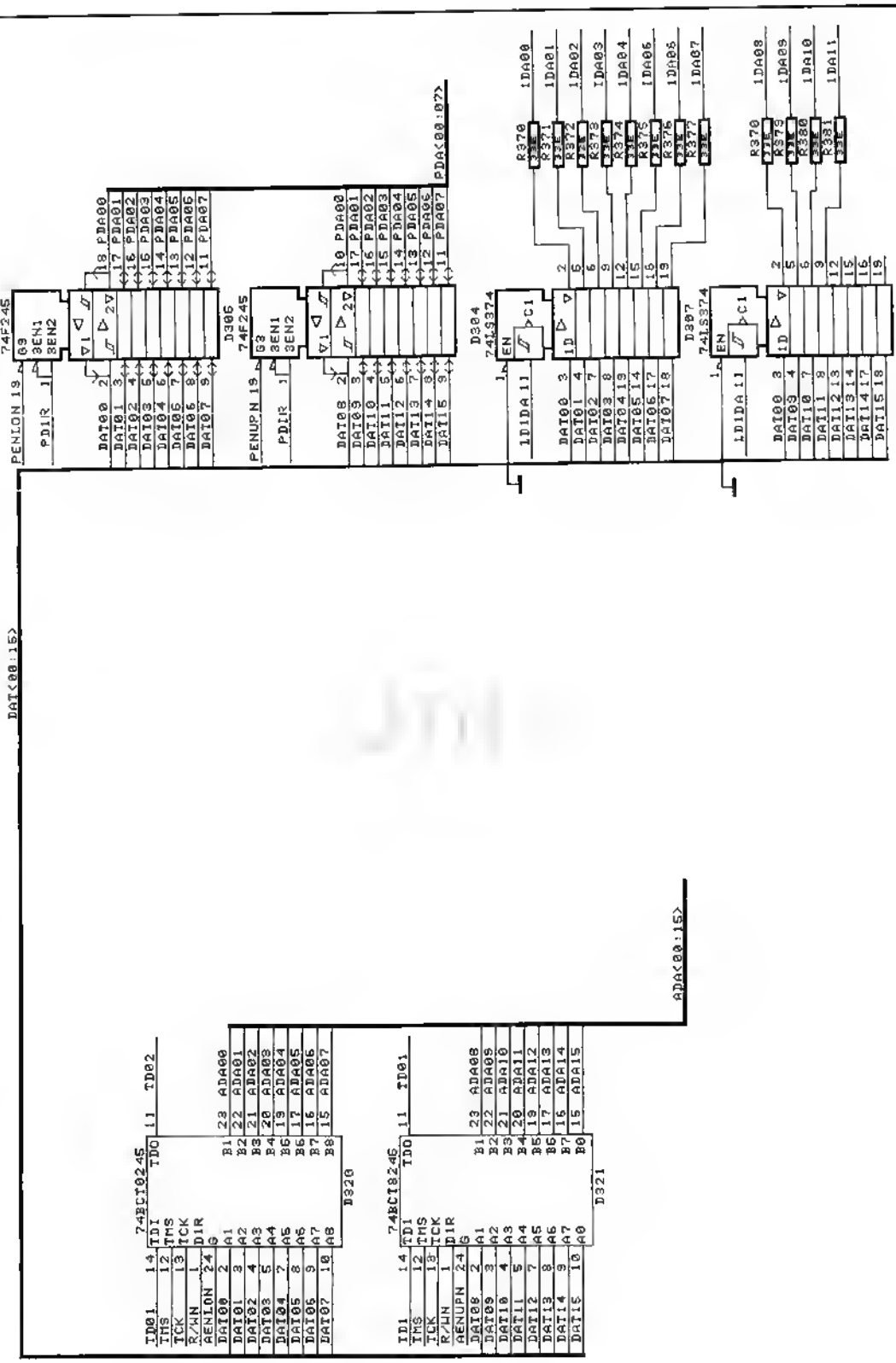


Fig. 3.20. Data bus buffers.

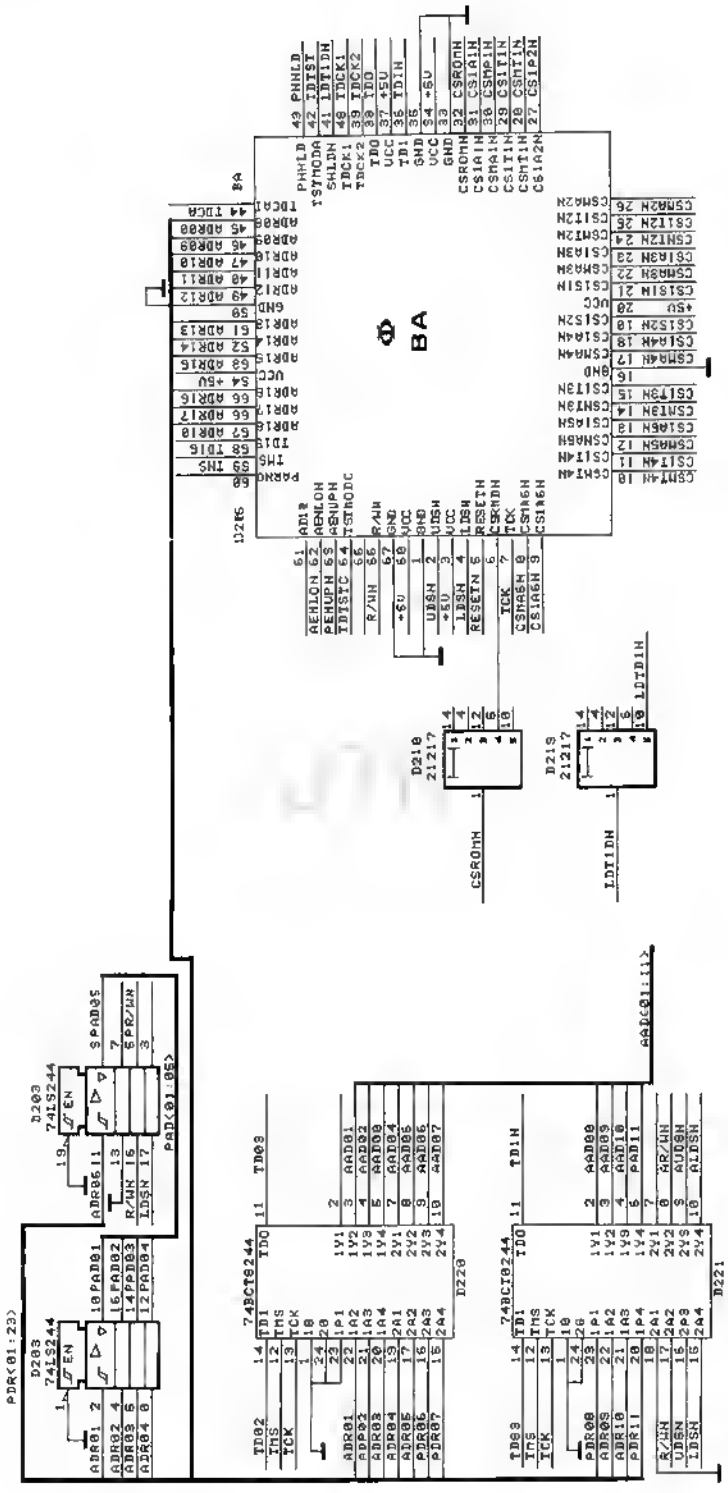


Fig. 3.21. Address bus buffers.

3.7.3.7 Peripherals.

The following peripherals are used:

- Floppy Disc Controller (FDC)
  Refer to Fig. 3.22.
- Centronics Parallel Controller
  Refer to Fig. 3.23.
- Multi Function Peripheral (MFP)
  Refer to Fig. 3.24.
- The GPIB controller (IEEE)
  Refer to Fig. 3.25.

The peripherals are stand alone circuits which are connected to the CPU by buffers on the data bus (D303 and D306) and address bus (D203) and they communicate with the CPU via interrupts and DMA requests.

Floppy Disk Controller (FDC).

The ***floppy disk controller*** D501 is the DP8473 packed in a PLCC. This chip is directly controllable by the CPU via the peripheral data and address bus. The chip is selected by GAL D500 pin 26 with signal CSFDCN, while read and write actions are controlled via pins 24 (write) and 25 (read) of the GAL. The FDC asserts a DMA request (FDREQ) when I/O actions with the floppy are desired. This signal is sent to the GAL which in turn sends a DREQ1N (DMA request 1) to the CPU. If the DMA request of the FDC is accepted, the CPU returns a DMA-acknowledge (DACK1N) to the GAL, and via pin 18 of the GAL the signal DAK is asserted to the FDC. Now a bus transfer of data to or from the system memory can be accomplished. Pin 33 of the FDC is used to indicate the completion of the transfer per block (DTC = Data Transfer Complete).
All timing of the FDC is controlled by its internal timing mechanism, via an external oscillator frequency of 24 MHz.
A Phase Locked Loop circuit (PLL) synchronises the incoming data on pin 44 (read data). Depending on the floppy density the appropriate PLL frequency is selected via filters R500 and C501 or R502 and C507.
All FDC signals from the floppy are directly (internally buffered) connected to the drive via connector X502.

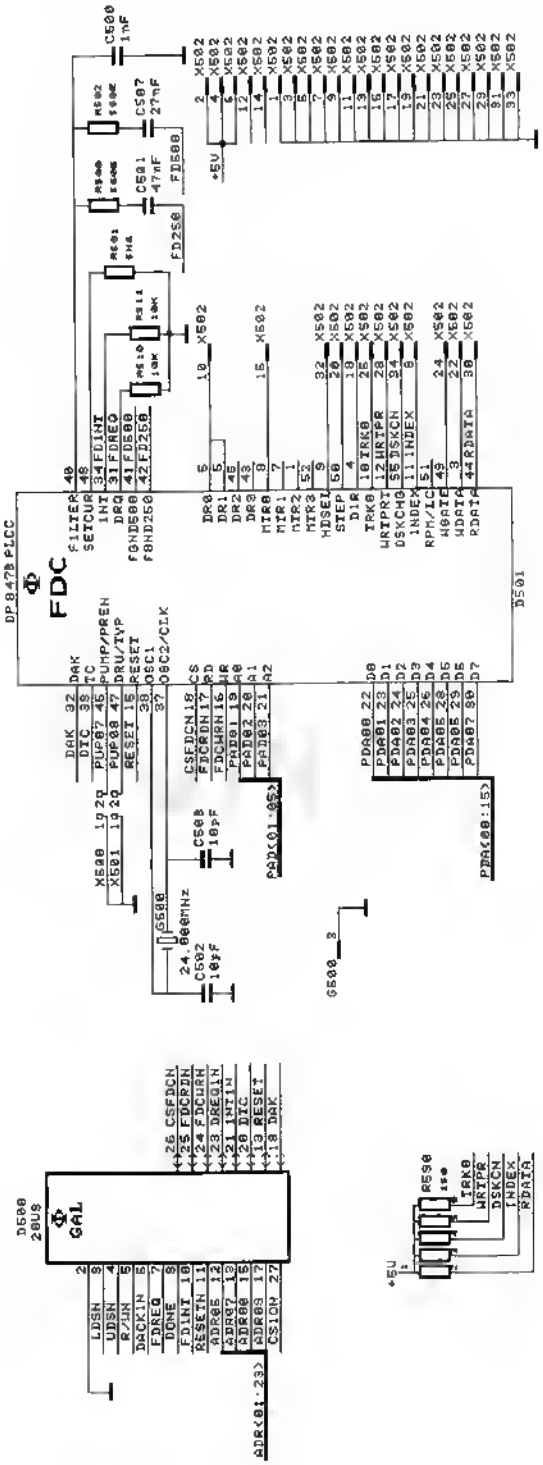


Fig. 3.22. Floppy disc controller.

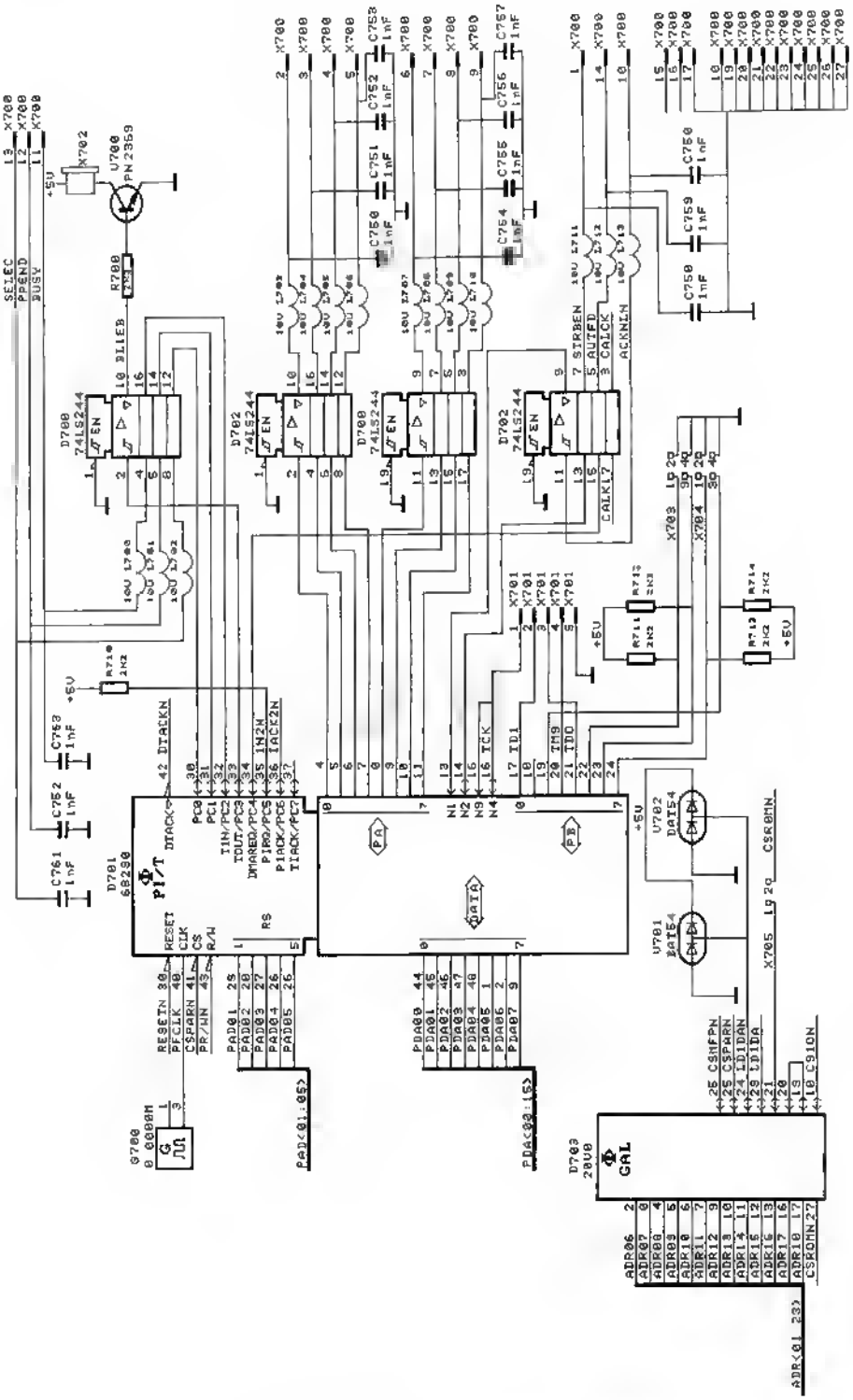


Fig. 3.23. Centronics parallel controller.

Centronics Parallel Controller.

IC D701 is the 68230 parallel interface and timer chip (PI/T).
The chip has 2 parallel ports (A and B). Port A is used as an 8 bit parallel output port. The 8 bits are buffered by D702 and D700 before they are sent to the printer connector X700.
Port B is partly used for boundary scan purposes (TDI, TDO and TMS), and partly as input to read the system board lay-out by the setting of the jumpers X703 and X704 (see also chapter 4.3.1 jumper settings).
Handshake is accomplished via signals H1 and H2 on pin 13 and pin 14.
GAL D703 selects with signal (CSPARN) on pin 25 the parallel controller, and with pin 26 (CSMFPN) the multi function peripheral (see next page).
The parallel controller has also a general purpose port C, which is used to guard the printer status (select, paper end and busy).
The communication with the CPU is based on interrupts (IN2N and IACK2N).
Every read and write action with the CPU is acknowledged by the parallel controller with pin 42 (DTACKN).

Multi Function Peripheral (MFP).

The MFP IC D601 (68901) has an on-chip USART, 4 timers and an 8 bit general purpose I/O port. The USART and 3 timers are intended for future use, while the I/O port is mainly intended as an interrupt control port, connected to the analyzer ASIC's.
GAL D600 divides the 8 MHz peripheral clock (PFCLK) by 2 and its output pin 26 is directly connected to the clock and Xtal input of the MFP.
The MFP communicates via interrupt signals IN4N and IACK4N with the 68070, and also asserts a DTACK (data transfer acknowledge) at every read and write action.
Pin 18 of the MFP delivers the calibration clock during the calibration mode of the analyzer.

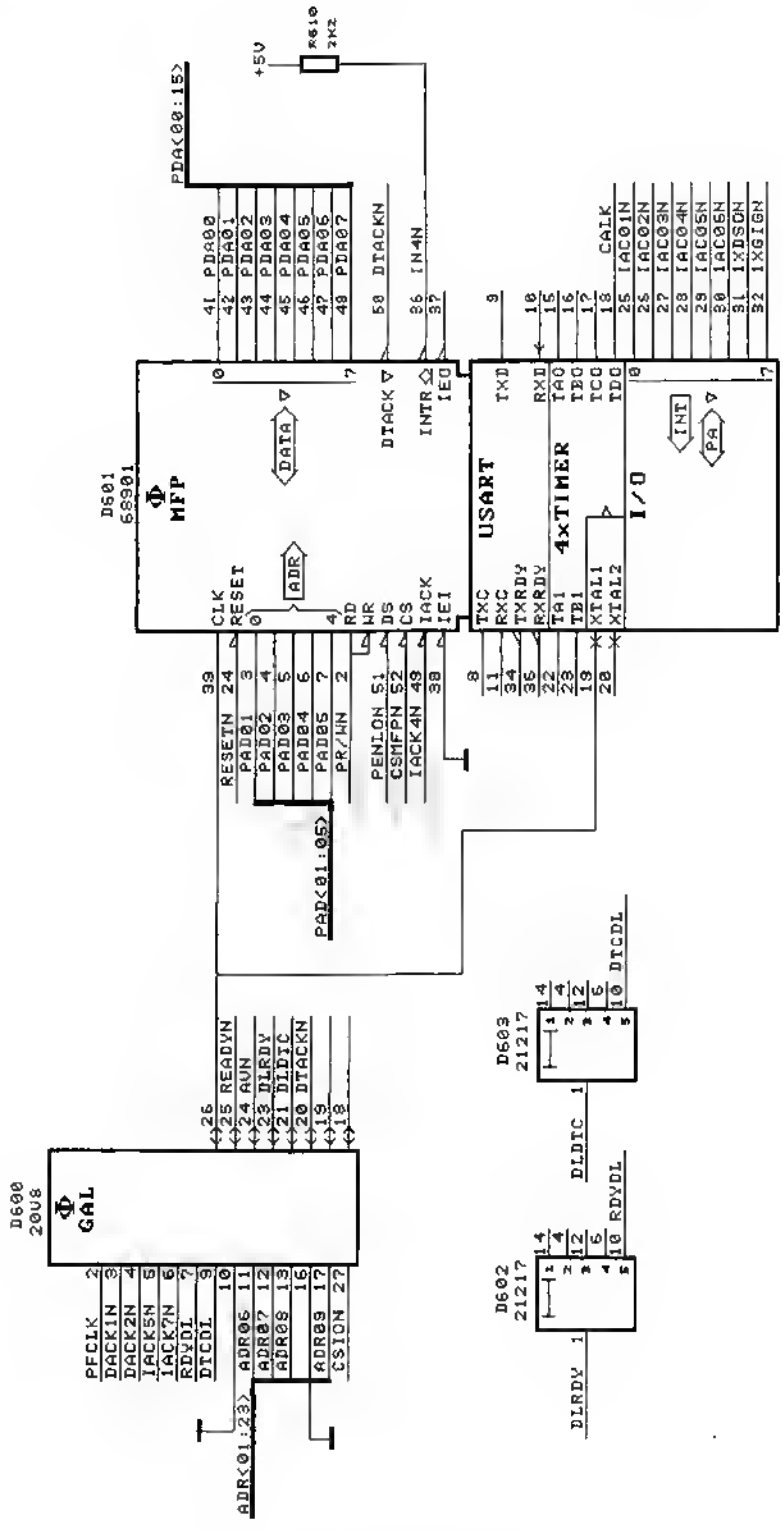


Fig. 3.24. Multi function peripheral.

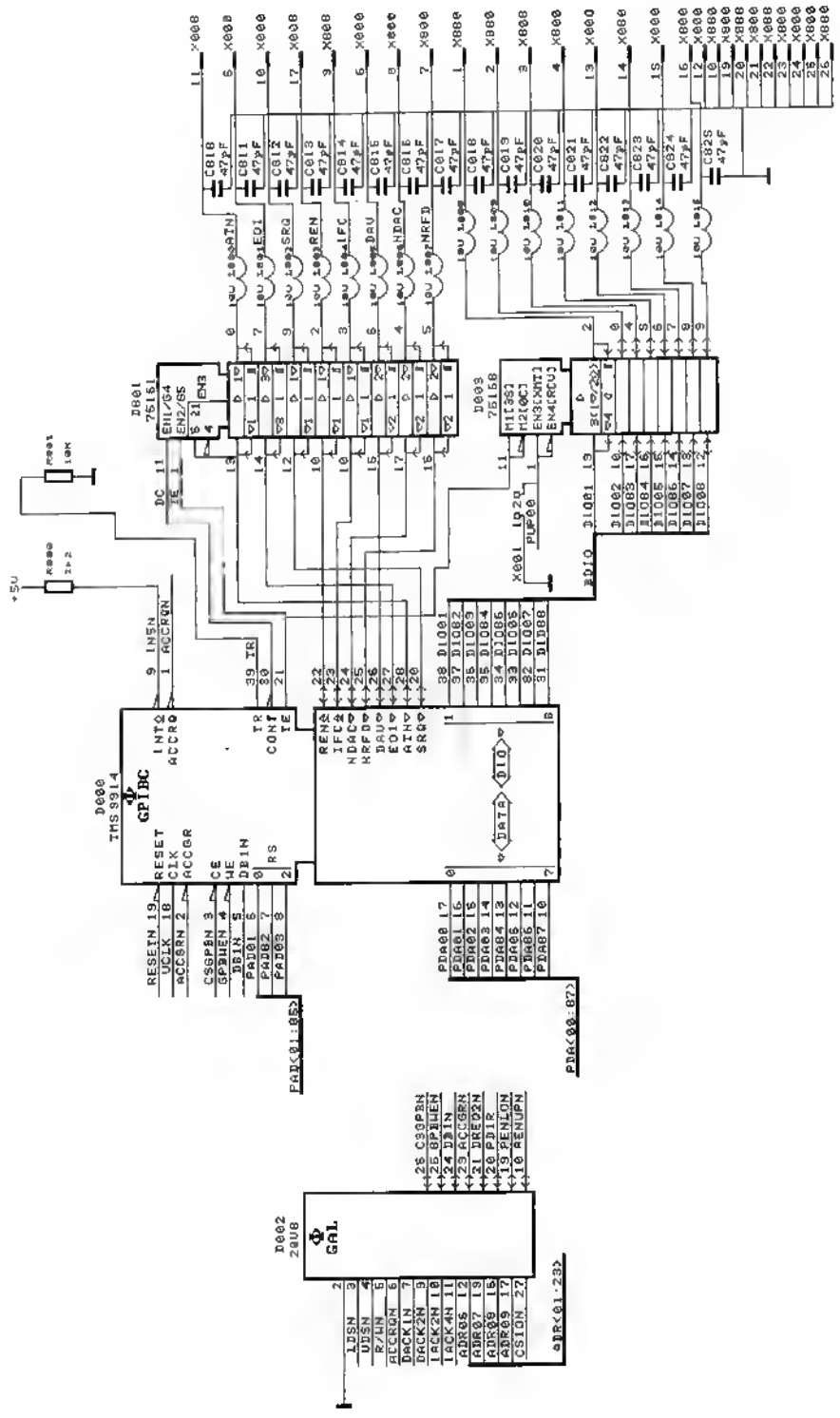


Fig. 3.25. GPIB controller.

The ***GPIB Controller*** (IEEE).

The TMS 9914 (D800) is the general purpose interface bus chip for ***IEEE control.***
X800 can be connected to an external IEEE bus. The IEEE hardware is not implemented but can optionally be installed on the main-board.
D800 is selected by GAL D802 (CSGPBN) pin 26. The communication to the CPU is done on interrupt base via the signal IN5N (pin 9 of D800).
D801 and D803 are bidirectional buffers to buffer the IEEE signals from and to X800.

3.7.4 Data Acquisition section.

3.7.4.1 General.

NOTE: **This section will not be explained in detail for competitive reasons. Information about the kernel of the data acquisition section will not be given. Extra information of this section is available on requeat at the Supply Centre.**
Only necessary information to understand the basic principle of the data acquisition section is given below.

The data acquisition system comprises Input ASIC's, Acquisition ASIC's, a Clock ASIC, Time ASIC's, Sequencer ASIC's and an interface to the CPU. There are two, four or six input sockets available for use on the 32/64/96 channel models respectively. Each input POD contains 16 input data lines. These can be used on state and timing applications simultaneously.

For state analysis the input signals are captured via a microprocessor adapter which is directly connected to a microprocessor pins to trace the clock, data, address, control signals, etc. Whereas supplementary timing probes can be connected to selected areas on the target board in order to collect information on the peripheral logic.

The inputs from the pods are passed into the Input ASIC's. There are two Input ASIC's dedicated to each input POD.

The Input ASIC's pass the data to the Acquisition ASIC's. The Acquisition ASIC's are clocked by the Clock ASIC.

To control the acquisition and storage, additional ASIC's such as Time and Sequencer ASIC's are required.

There are four basic models of the analyzer available:

PM 3580/30 32 channel 100 MHz
PM 3580/60 64 channel 100 MHz
PM 3585/60 64 channel 200 MHz
PM 3585/90 96 channel 200 MHz

The number of ASIC's for the various models of analyzer's are as follows:

ASIC	86Ch. 200 MHz	64Ch. 200 MHz	64Ch. 100 MHz	32Ch. 100 MHz
Input	12	8	8	4
Acquisition	6	4	4	2
Time	4	4	1	1
Sequence	2	2	1	1
Clock	1	1	1	1

ASIC's used for each model are:

PM 3580/30, 32 channel 100 MHz

- Input D1, D2, D3 and D4
- Acquisition D5000 and D5001
- Time D5009
- Sequence D5020
- Clock D6000

PM 3580/60, 64 channel 100 MHz

- Input D1, D2, D3, D4, D5, D6, D7 and D8
- Acquisition D5000, D5001, D5002 and D5003
- Time D5009
- Sequence D5020
- Clock D6000

PM 3585/60, 64 channel 200 MHz

- Input D1, D2, D3, D4, D5, D6, D7 and D8
- Acquisition D5000, D50001, D50002 and D5003
- Time D5006, D5007, D5009 and D5010
- Sequence D5020 and D5021
- Clock D6000

PM 3585/90, 96 channel 200 MHz

- Input D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11 and D12
- Acquisition D5000, D5001, D5002, D5003, D5004 and D5005
- Time D5006, D5007, D5009 and D5010
- Sequence D5020 and D5021
- Clock D6000

3.7.4.2 Data Input.

A group of 8 channels is passed to a single input ASIC. The diagram in Fig. 3.26 shows the overall data path from probe tip to input ASIC for one channel only.
Input ASIC's D1 to D12 are software controlled by the CPU section and have 2 modes:

* Calibration mode.
* Normal mode

In the ***calibration mode*** a calibration clock is passed from the MFP (D601 pin 18) to buffer D702, to the TTL/ECL converter D6003 and to ECL buffer D6001 (refer to Fig. 3.27).
This buffer will output the CAL clock via 6 Buffered outputs (VCAL1 to VCAL6).
The VCAL1 signal is connected to ASIC's D1 and D2, VCAL2 is connected to D3 and D4, etc.

Calibration is performed during start-up of the instrument. During calibration the Acquisition ASIC's are programmed in such a way that all data channel coming from the Input ASIC have the same behaviour (hold-time performance).
If the calibration is not OK, (channels could not be programmed to be equal), the message "Calibration failed" appears.
In this condition the not calibrated channels can behave differently i.e. they contain a particular skew in comparison to the calibrated channels.
The instrument can however still be used keeping the failure in mind.

Calibration failed can have several causes:

1. Pins of the Input ASIC's are loose or not proper connected. (Visual inspection)
2. The above mentioned calibration signal path is interrupted or disconnected. (Check this with an oscilloscope during calibration.)
3. Input ASIC is defective. (Check with the logic target PF 8669/20 and an oscilloscope the input circuitry from POD input to Input ASIC's output.)
4. Acquisition ASIC's are defective. (Find defective AA with BST-diagnostics).

Please check upon above mentioned items when calibration fails.

When the input ASIC is programmed in the normal mode, the 8 inputs are passed to the 8 outputs.
Also a single input line can be used as a state clock, in which case this channel is available at the pins 19 or 20 of that input ASIC, to serve as a master state clock for the analyzer.

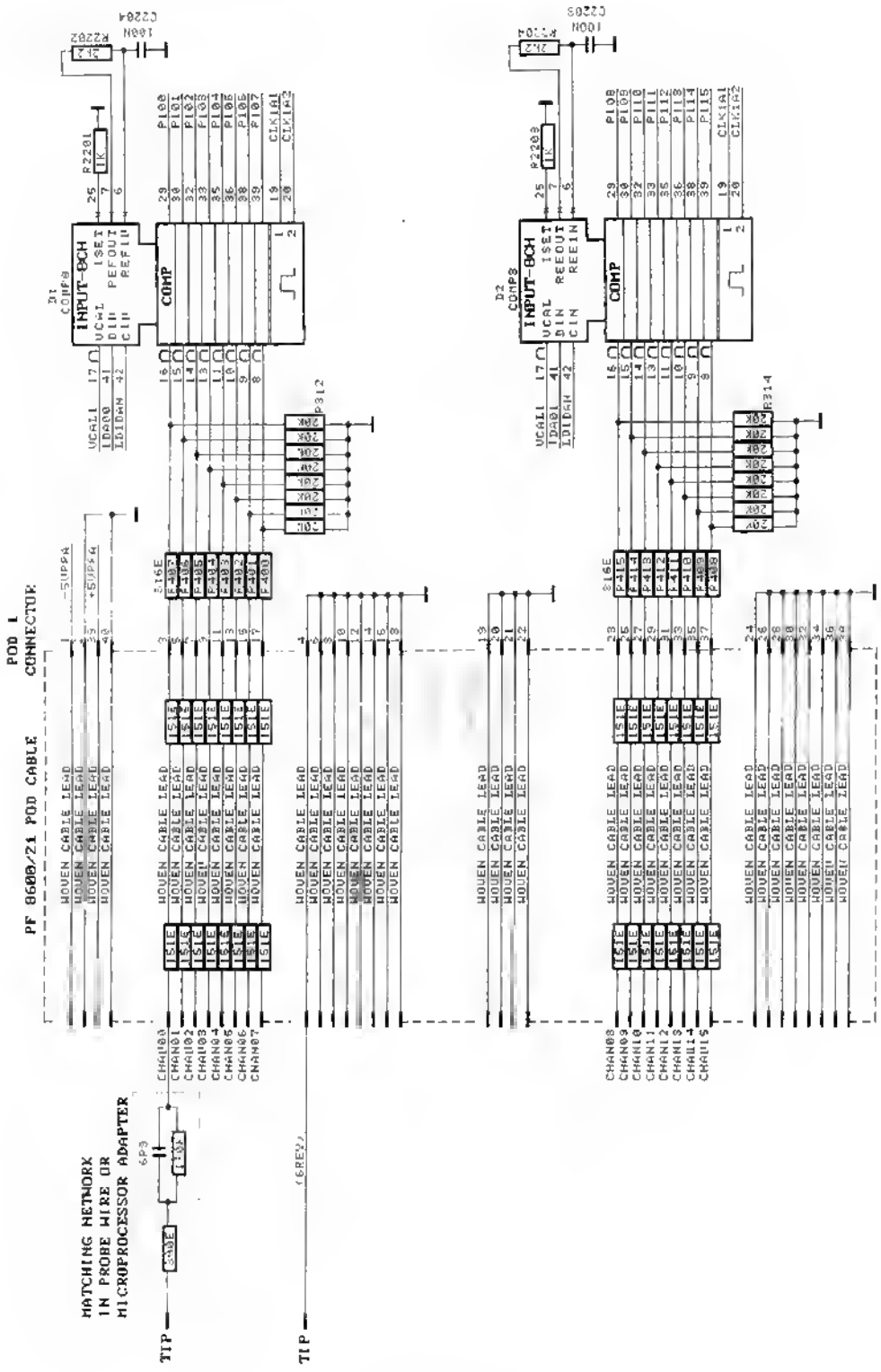


Fig. 3.26. Data input.

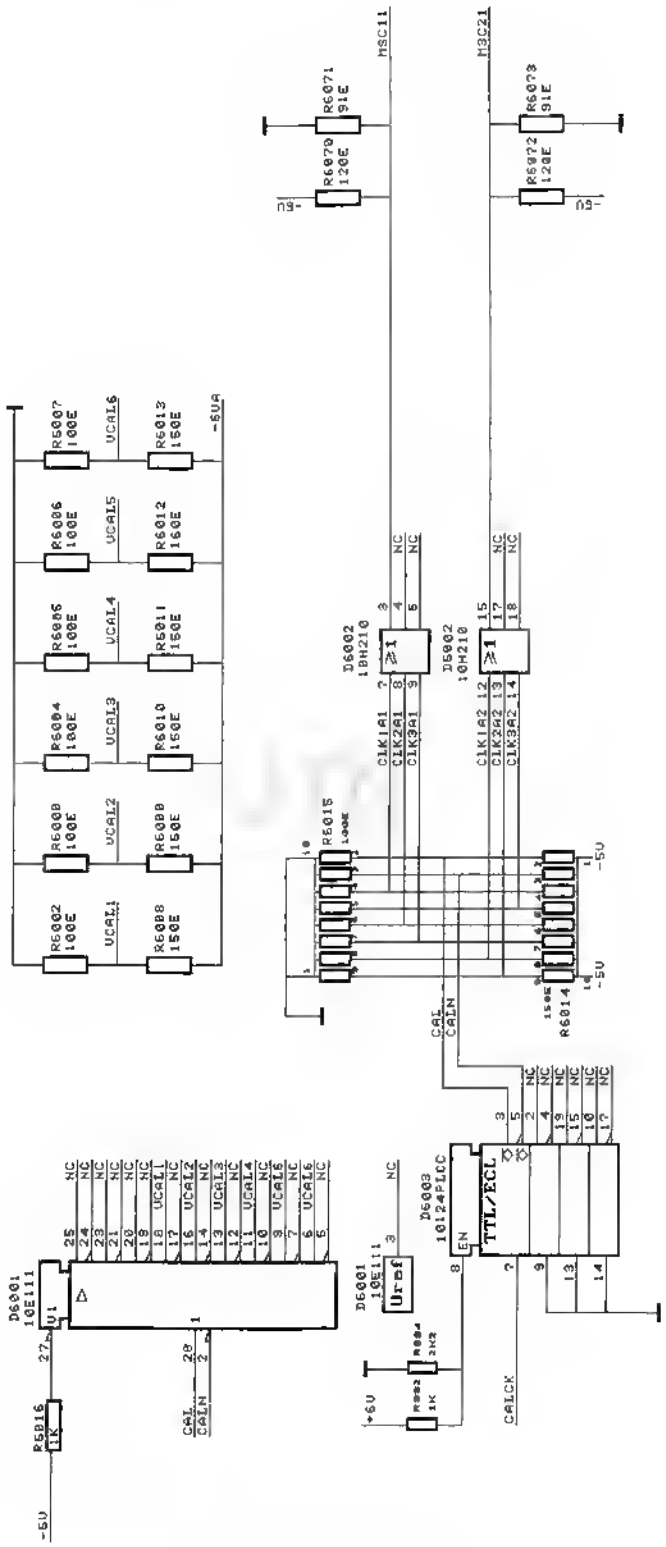
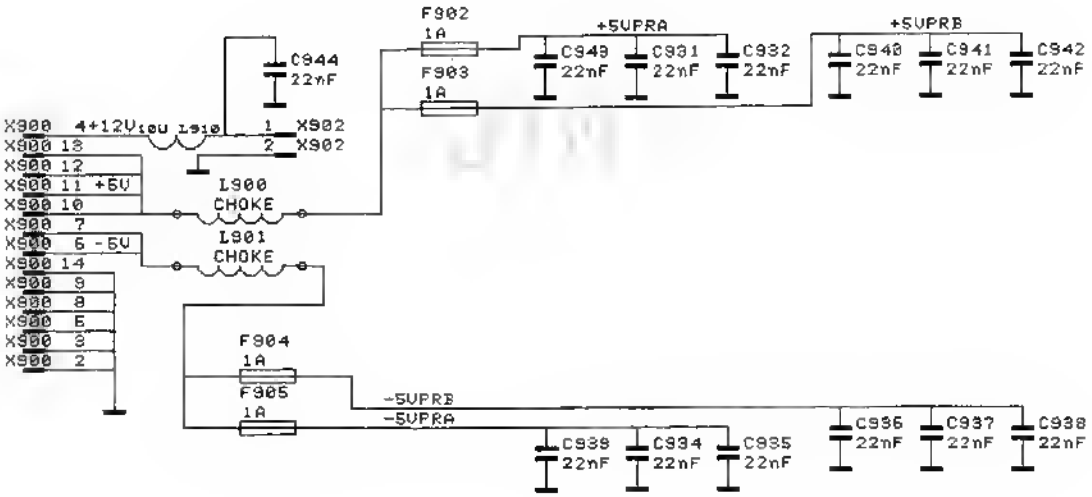
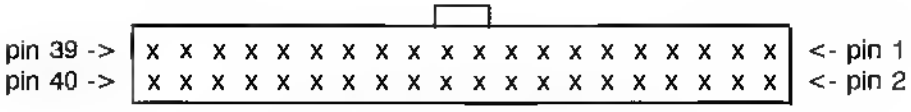


Fig. 3.27. Calibration circuit.

3.7.4.3 POD Power Supply.

Each Pod connector at the front of the analyzer supplies a +5V and a -5V power for external use (i.e. the logic target).
These voltages are directly supplied by the power supply and are secured by the reset-able over-current protectors F902, F903, F904 and F905. This fuse protects as soon as its internal temperature rises above the "trip-temperature" (125°C). In an overload situation the "trip-temperature" will be reached and the internal resistance of the component will change rapidly from about 0.2 Ohm to factors of ten of this value. The fuse will recover automatically when the overload disappears.
F902 will protect the +5VPRA voltage, which is connected to pin 39 of all odd PODs.
F903 will protect the +5VPRB voltage, which is connected to pin 39 of all even PODs.
F904 will protect the -5VPRA voltage, which is connected to pin 1 of all odd PODs.
F905 will protect the -5VPRB voltage, which is connected to pin 1 of all even PODs.





All even pins are connected to ground

Fig. 3.28. POD input connector.

3.7.4.4 External Trigger Control.

The analyzer Trig-in and Trig-out BNC connectors at the rear of the instrument are both buffered. An input pulse to the analyzer is buffered by D7000 and send to D7001 to create the inverted pulse TRINP for the sequencer ASIC.
An output pulse from the analyzer is generated by the sequencer ASIC of analyzer 1 (BNC01) or the sequencer ASIC of analyzer 2 (BNC02). Both signals are ORed in D7001 and then buffered by D7000 before the pulse appears on the output of X7000.

3.7.4.5 Main-board Temperature Guarding.

The main-board ambient temperature is sensed continuously by switch S7011.
This switch will short pin 1 of X900 to ground, whenever the ambient temperature rises above the 70°C.
Pin 1 of X900 is connected to the protection circuit of the power supply (See chapter 3.12).
An overheating will immediately shut down the power supply.

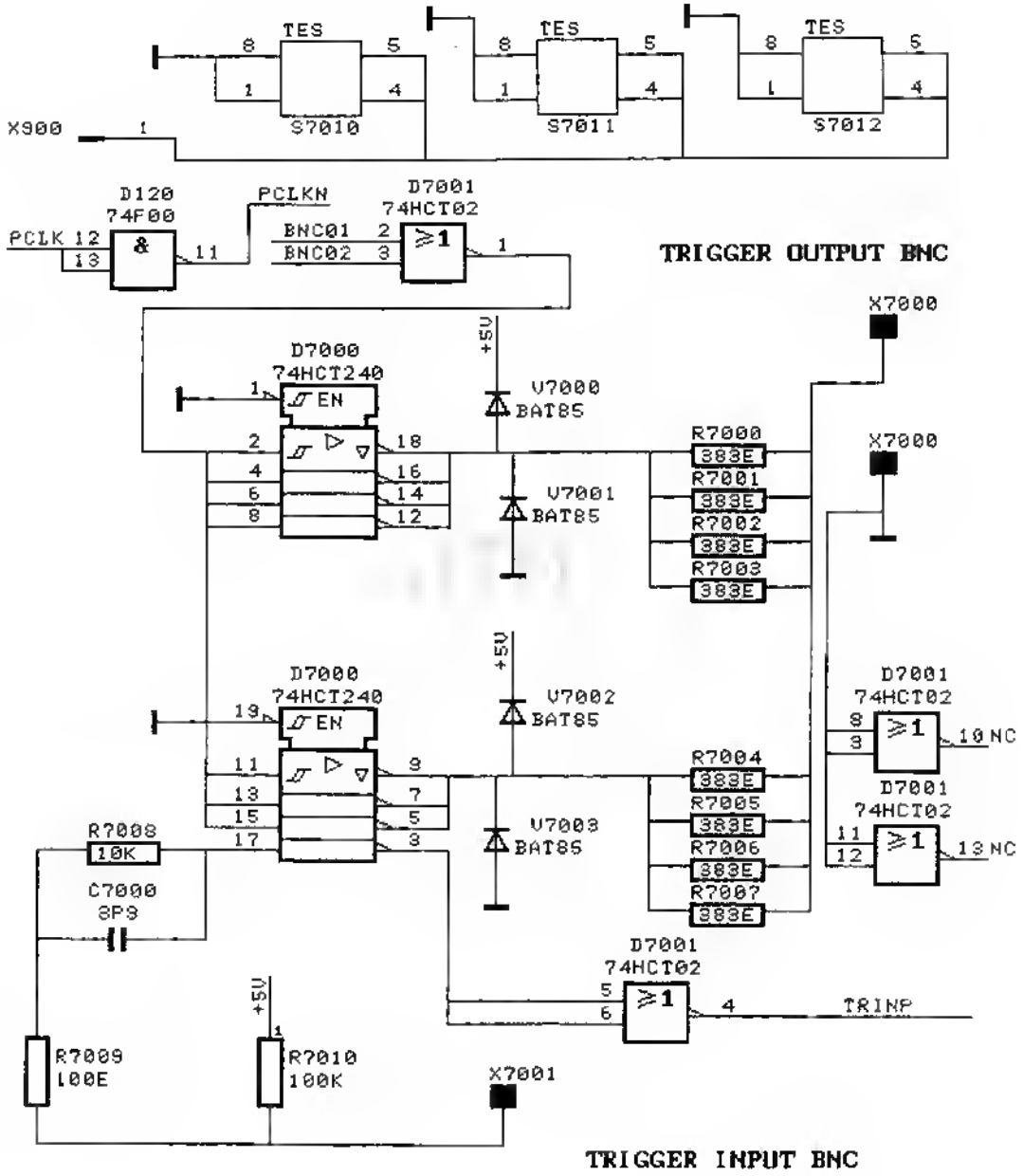


Fig. 3.29. Trigger control circuit.

NOTE.

CHAPTER 4.

4. VARIOUS ADJUSTMENTS AND JUMPER SETTINGS.

CONTENTS.

4.1 GENERAL INFORMATION.

This section contains all the ***adjustment information*** and ***jumper settings*** necessary to maintain the performance of the PM 3580 and PM 3585 series of Logic Analyzers. Before any adjustment the equipment must attain its normal operating temperature.

Before starting the alignments the following must be noted:

- The warm-up time under normal operating conditions is 15 minutes.
- Where possible, instrument performance should be checked before any adjustment is made.
- All limits and tolerances given in this section are guides, and should not be interpreted as instrument specifications unless they are also published in chapter 8 of this manual.
- Tolerances given are for the instrument under test and do not include test equipment error.
- The most accurate display adjustments are made with a stable, well-focused low intensity display.
- All controls that are mentioned without item numbers are located on the outside of the instrument.

WARNING: THE OPENING OF COVERS OR REMOVAL OF PARTS, EXCEPT THOSE TO WHICH ACCESS CAN BE GAINED BY HAND, IS LIKELY TO EXPOSE LIVE PARTS, AND ALSO ACCESSIBLE TERMINALS MAY BE LIVE.

THE INSTRUMENT MUST BE DISCONNECTED FROM ALL VOLTAGE SOURCES BEFORE COMMENCING ANY REPLACEMENT, MAINTENANCE OR REPAIR PROCEDURE THAT REQUIRES THE INSTRUMENT TO BE OPENED.

WHEN IT IS NECESSARY THAT VOLTAGE MUST BE APPLIED TO AN OPEN INSTRUMENT IN ORDER TO CARRY OUT A TASK, THEN THE TASK MUST ONLY BE PERFORMED BY A QUALIFIED PERSON THAT IS AWARE OF THE HAZARDS INVOLVED.

BE AWARE THAT CAPACITORS INSIDE THE INSTRUMENT MAY STILL HOLD A CHARGE AFTER THE INSTRUMENT HAS BEEN DISCONNECTED FROM A VOLTAGE SOURCE.

4.2 ADJUSTMENT PROCEDURES.

4.2.1 POWER SUPPLY ADJUSTMENT.

To gain access to the power supply board refer to chapter 2 of this manual.

NOTE:
1. Disconnect and remove the power supply from the mainframe.
2. Use an external fan to cool the power supply
3. The loadings for adjustment of the power supply must be:

+ 5V	10 A
+12V	1 A
- 5V	1.5A

4. The input voltage used for adjustments of the power supply must be 230V (or 115V).

WARNING: **Use an isolation transformer when maintaining the power supply. Be aware of hazards involved, included charged capacitors, after switching off the power supply.**

The power supply must be adjusted in the following order:

1. +5V over-voltage setting with potentiometer VR3.
2. +5V output voltage setting with potentiometer VR2.
3. -5V over-voltage setting with potentiometer VR4.
4. +12V output voltage setting with potentiometer VR1.
5. Maximum total power setting with potentiometer R26.

After the adjustment the following items should be checked:

1. +12V over-current protection.
2. -5V over-current protection.
3. Remote controlled shutdown.

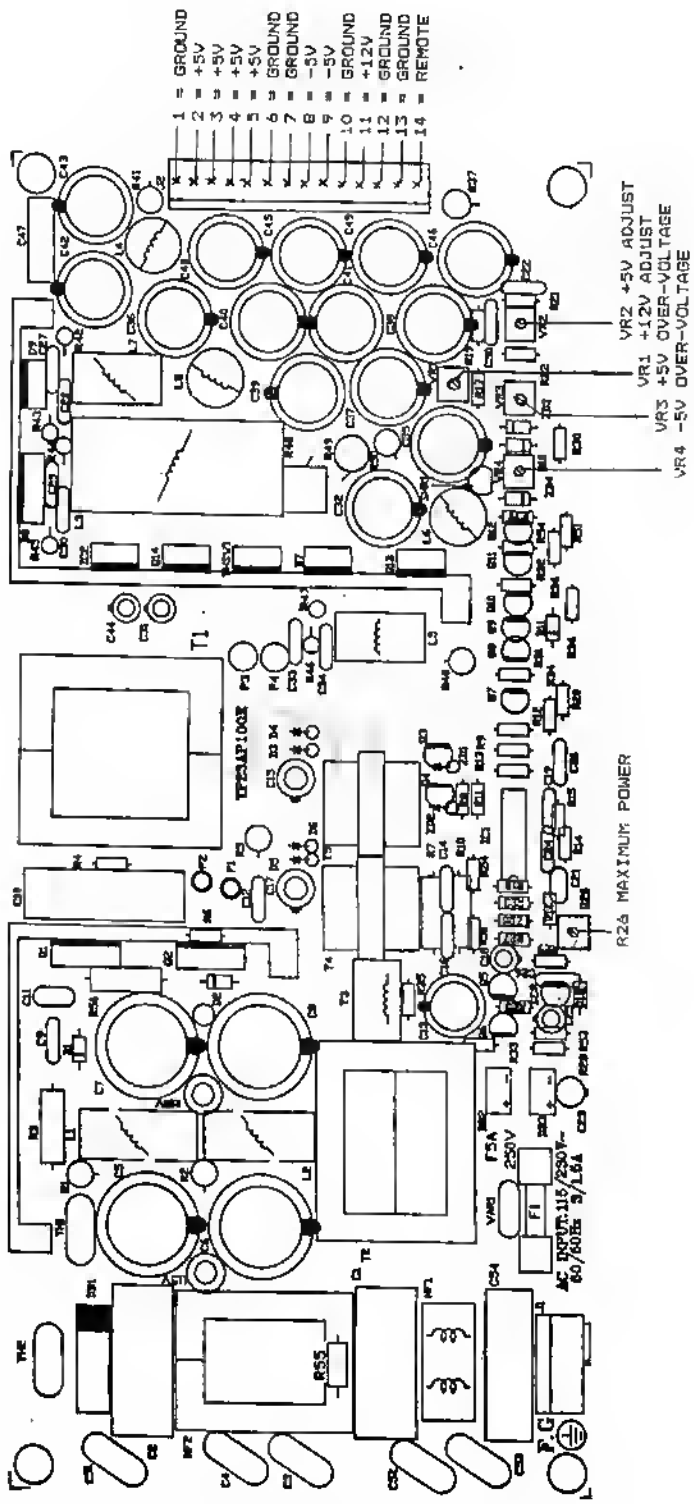


Fig. 4.1. Power supply adjustment.

+5V over-voltage setting.

1. Connect a digital voltmeter between the +5V output and ground of J2.
2. Turn VR3 fully counter clock-wise (protection > 7V).
3. Turn VR2 counter clock-wise to read on the voltmeter +6V.
4. Now slowly turn VR3 clock-wise until the power supply switches off. Leave VR3 in this position.
5. Turn VR2 fully clock-wise to reduce the +5V output, enabling the power supply to start up next time.
6. Switch off the mains-voltage and let the circuits recover for about 20 seconds.
7. Readjust the +5V. See below.

+5V output voltage setting.

1. Connect a digital voltmeter between the +5V and ground of J2.
2. Adjust with potentiometer VR2 the meter reading to +5.05V $\pm$ 20 mV.

-5V over-voltage setting.

1. Connect a digital voltmeter between the -5V output and ground of J2.
2. Turn VR4 fully counter-clockwise.
3. Connect the -5V lead of the external power supply to the -5V output of J2, and the return lead to the ground of J2. (Use a current setting of approx 1A.)
4. Set the external power supply to -6V $\pm$ 20 mV.
5. Now slowly turn VR4 clock-wise until the power supply switches off. Leave VR4 in this position.
6. Remove the external power supply.
7. Switch off the mains-voltage and let the circuits recover for about 20 seconds.

+12V output voltage setting.

1. Connect a digital voltmeter between the +12V and ground of J2.
2. Adjust with potentiometer VR1 the meter reading to +12V $\pm$ 40 mV.

Maximum total power setting.

The total power used by the power supply may not exceed a maximum value, if the maximum value is exceeded, the power supply must switch off.

Warning: This adjustments must be done with sufficient cooling. Also heavy conductor leads must be used due to the large amount of current involved.

To adjust this maximum setting proceed as follows:

1. Turn R26 fully counter-clockwise.
2. Load the +5V with 28A, the +12V with 2A and the -5V with 3A.
3. Slowly turn R26 clockwise until the power supply switches off.
4. Leave R26 in this position.
5. Switch off the mains-voltage, remove the maximum loads and let the circuits recover for about 20 seconds.

4.2.2 POWER SUPPLY CHECKING.

+12V over-current protection.

This over-current protection circuit is not adjustable but must act if the +12V load rises above 3.8A $\pm$ 0.2A.

-5V over-current protection.

This over-current protection circuit is not adjustable but must act if the -5V load rises above 4.2A $\pm$ 0.2A.

Remote controlled shutdown.

The power supply must shutdown immediately if pin 14 (REMOTE) of J2 is short to ground.

If the above mentioned functions do not work properly then the involved parts must be checked on tolerance and specifications.

4.2.3 ADJUSTMENT OF THE MONITOR.

WARNING: BE CAREFUL NOT TO TOUCH THE HIGH VOLTAGE ON THE VARIOUS PRINTED CIRCUIT BOARDS.

DO NOT ALIGN THE MONITOR IN THE VICINITY OF ANY IRON OBJECTS SUCH AS CENTRAL HEATING RADIATORS ETC.

ONLY USE PLASTIC ALIGNMENT TOOLS.

The position of the components to align are as follows:

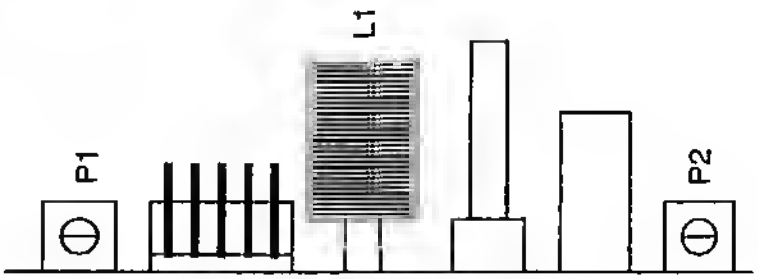


FIG. 4.2. Video display adjustment.

The ***monitor alignment*** procedure should be completed in the following manner.

1. Set the brightness control on the rear of the instrument to a position where the black edges just outside the video picture on the screen don't light up.

2. With the help of the VSC test on the diagnostic diskette the focus must be set to maximum picture sharpness using the potentiometer P2 on the video control board. Use the dots in the edges of the screen as a reference.

3. If the picture is not positioned perfectly horizontally then the screen can be adjusted by turning the deflection coil.

In order do this:

a) Loosen the screw on the deflection coil.

b) Keep the coil tight against the rear of the picture tube.

c) Turn the coil at the rear of the picture tube to correct the horizontal alignment.

Fig. 4.3. Horizontal alignment.

d) Tighten the screw.

WARNING: DO NOT FASTEN THE SCREW TOO TIGHTLY. THIS COULD DAMAGE THE PLASTIC AND THE PICTURE TUBE.

4. The picture must now be centred. The VSC test on the diagnostic diskette can be used. The display in this test has a small grey box located in its centre. The location of the exact centre is 9,00 cm (2.36 inch) from the left edge of the screen and 6,85 cm (2.7 inch) from the lower edge of the screen.

To locate the display in the centre of the screen the two ***magnetic rings*** on the neck of the deflection coil can be aligned. The rings can be moved together or individually. Each of the rings has a tip to enable it to be turned. Set both of the tips together and then turn both of the rings at the same time. This will move the picture about the screen in a circular motion with a fixed radius (R). By turning the two rings in an opposite direction to each other, radius R can be changed. Change R so that the display at the centre of the screen has minimum movement when both of the rings are moved together. Position the centre of the display to the exact centre of the screen by moving the two rings together about the deflection coil.

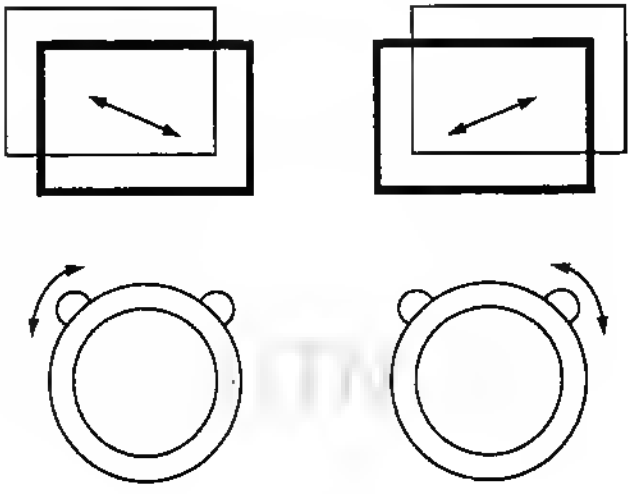


Fig. 4.4. Screen centre adjustment.

5. The height must now be adjusted with the potentiometer P1. Because the ***screen corner corrections*** are not yet aligned look to the exact middle of the horizontal top line of the picture. Set this line to the top edge of the screen. If alignment 4 has been done correctly also the bottom line now will touch the bottom edge of the screen.

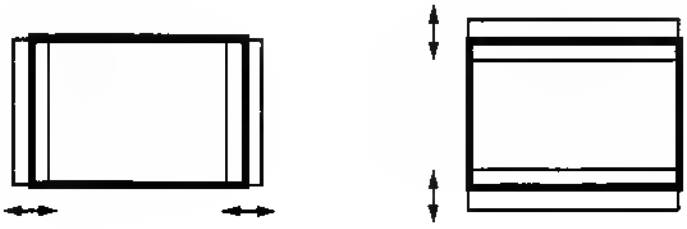


Fig. 4.5. Screen width & height correction.

The width of the picture must be aligned using coil L1. In this procedure the middle of the video picture must meet both's middle of the left and right screen edges. Note that it might be necessary to repeat the procedures 4 & 5 until a satisfactory result is achieved.

6. The last adjustment is that for corner correctness, this is better known as ***pin cushion and barrel correction***. Magnets are available on the edges of the deflection coils to correct the deflection at each screen corner. Each magnet can be turned and shifted in a circular motion on the deflection coil edge. By turning the magnet around on its own position the position of the picture spot will move along a diagonal of the screen. Shifting the magnet will move each picture spot in the corner. In a circular manner rectangularly on the diagonal.

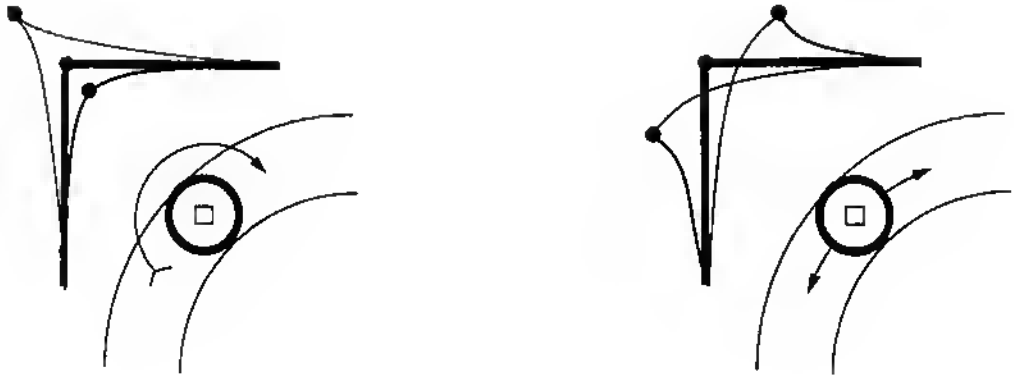


Fig. 4.6. Screen corner corrections.

4.2.4 ADJUSTMENT OF THE REAL TIME CLOCK.

In order to align the Real-Time clock a Frequency/Time meter is required. The time can be aligned using C109. By adjusting C109 the output pulse on pin 7 of IC D110 must be set exactly to a period time of 1 second. Only use a plastic trimming tool to complete this procedure.

A rough adjustment of the Real-Time clock can be made without the use of a meter by setting C109 to half of its capacity. This will result in a misalignment of 0.2 ppm, this is approximately one second in two months.

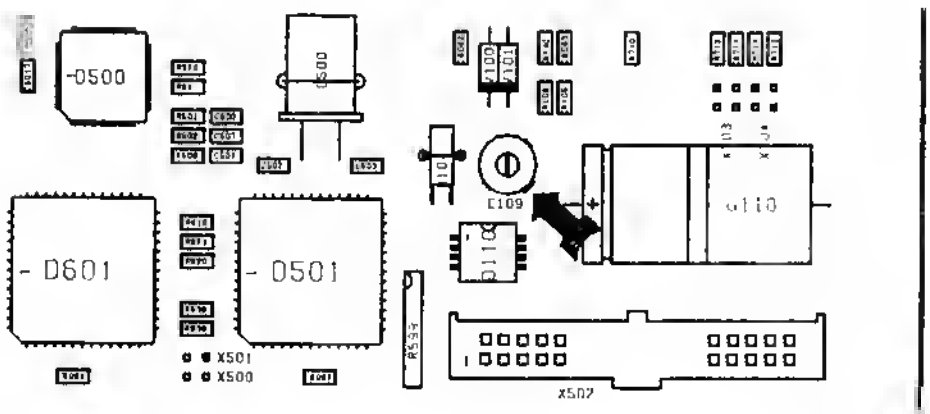


Fig. 4.7. Real time clock adjustment.

4.3 JUMPERS AND CONNECTORS.

Jumpers and connectors are used on the 100 MHz as well as on the 200 MHz boards:

X1, X2, X3, X4, X5, X6	Input PODS
X100	***RS-232 output port***
X101	***Keyboard input connector***
X102	***Video output connector***
X103	***MVGA output***
X104	Video display background setting
X105	Reset for CPU part
X402	***EPROM type selection***
X500	Select external data separator
X501	Drive control signals level type
X502	***Floppy drive connector***
X700	***Centronix parallel output***
X701	***BST connector*** (external)
X702	Beeper
X703	Hardware ***board type selection***
X704	Hardware ***board type selection***
X705	Chip select PROM
X800	***IEEE connector***
X801	IEEE transmit/receive disabling
X900	***Power supply connector***
X902	***Fan unit connector***
X5000, X5001, X5002, X5003	***BST chain jumpers***
X7000	***BNC trigger output***
X7001	***BNC trigger input***

4.3.1 JUMPER SETTINGS.

There are no jumpers used on the POWER SUPPLY, VIDEO MONITOR and KEYBOARD.
To locate the jumpers on the main board, face the board with the POD connectors towards you.

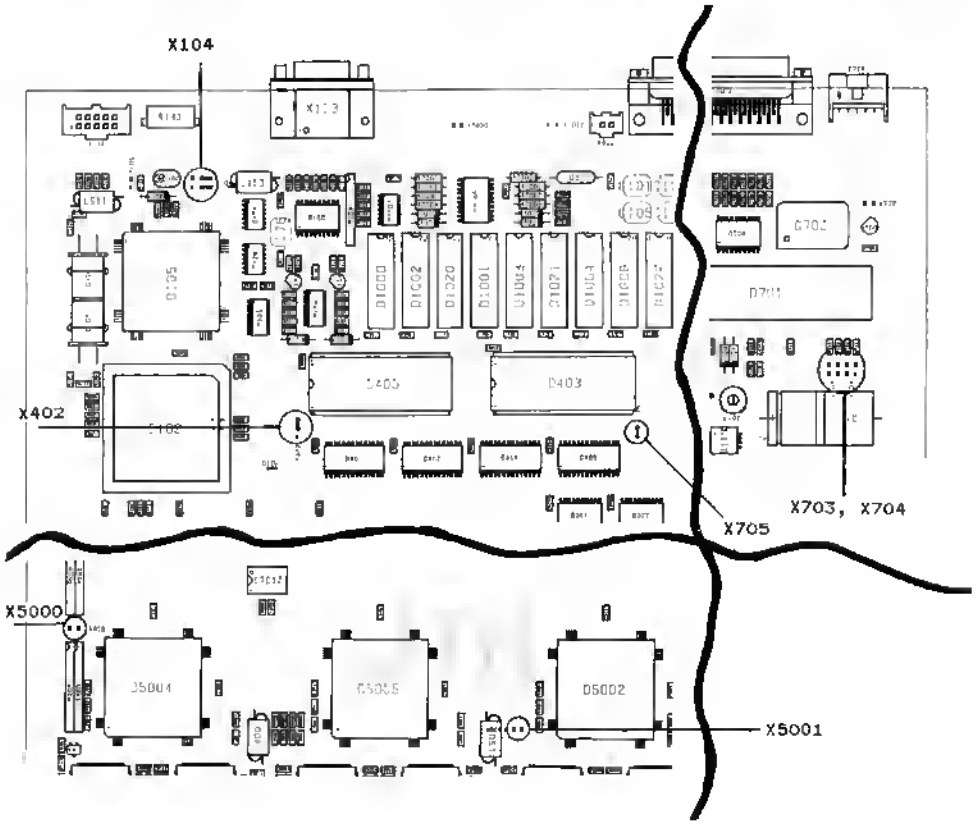


Fig. 4.8. The jumpers to be set on the main-board.

X104 - Video background setting.

X104
o---o o
o---o o
Black background
& White letter

X104
o o---o
o o---o
White background
& Black letter

X402 - EPROM TYPE OF D400, D403.

X402
o
|
o

o
27C010 & 27512 EPROM

X402
o

o
|
o
27256 EPROM

X500 and X501 FLOPPY DISK CONTROLLER.

	X500	X501
Not used	o o	o o

X703 and X704 - BOARD TYPE SETTING.

	X703	X704
200 MHz 96 channels	o o o o	o o o o
200 MHz 64 channels	o o o o	o o | o o
100 MHz 64 channels	o o | o o	o o | o o
100 MHz 32 channels	o o | | o o	o o o o

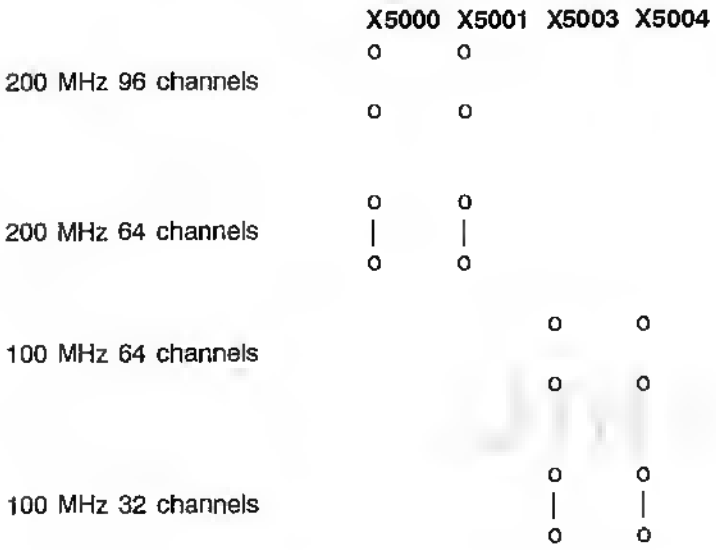
X705 - Chip select PROM.

X705	
o | o	always present

X801 - IEEE TRX/RDX DISABLING.

X5000, X5001, X5002 and X5003 - Boundary Scan.

NOTE: On the 200 MHz boards X5002 and X5003 do not exist and on the 100 MHz boards X5000 and X5001 do not exist.



NOTES.

CHAPTER 5.

5. ADAPTORS.

CONTENTS.

5.1 INTRODUCTION.

Data to be acquired is applied to the POD input of the logic analyzer via an adaptor connected onto the target system.

There are two types of adaptors:

Timing Adaptors - Generally used for timing measurements in various logic circuits with loose probes.

uProc. Adaptors - Used for data acquisition directly from the target microprocessor.

An adaptor is connected, via a 40 wire woven cable to the POD input of the analyzer.

The 40 wires consist of:

16	Signal wires
18	Ground wires (AC)
2	Not used wires
1	+5V wire (100 mA max.)
1	-5V wire (100 mA max.)
2	Ground wires (dc)

Each of the signal leads has a matching impedance of 151 Ohm at each end of the lead.

5.1.1 TIMING ADAPTORS.

A timing adaptor is clipped onto the woven cable. On the timing adaptor measuring probes are connected together with four earth leads. There are short and long earth leads. The long leads can be used generally, but for high frequency measurements the short leads are recommended, and should be connected as close as possible to the target measure spot. In each measuring probe lead a special matching network is integrated.

5.1.2 MICROPROCESSOR ADAPTORS.

Microprocessor adaptors are available for the most commonly used microprocessors. These adaptors can be passive (no electronics) or active (with electronics). Adaptors are particulary suitable for the acquisition of state information which can be converted into assembler mnemonics (disassembly).

According to the adaptor used, a software disassembler can be loaded, which automatically set up the FORMAT menu with the correct labels and signals.

Connection to the microprocessor under test is possible in three ways:

1 Connecting timing probes of a timing adaptor via the grey, low profile mini measuring clips. This means that every signal must be assigned manually in the FORMAT menu.

2 Via a multi-pin measuring clip (40 pins etc.) that fits on the microprocessor under test. On this clip, timing probes (without mini measuring clips) can be CONNECTED. Here also, every signal must be assigned manually in the FORMAT menu.

3 The microprocessor of the system under test is removed and inserted in the socket of a microprocessor adaptor. (The adaptor can be connected to the system under test via a "low profile" connector when the space above the micro-processor is limited.) On loading the proper disassembler, every connection pin of the adaptor is automatically defined in the FORMAT menu.

The adaptor ground wire must always be connected to a suitable ground point close to the circuit under test.

5.1.3 OVERALL SIGNAL PATH.

The overall signal path per lead for both a timing adaptor and a microprocessor adaptor is as follows:

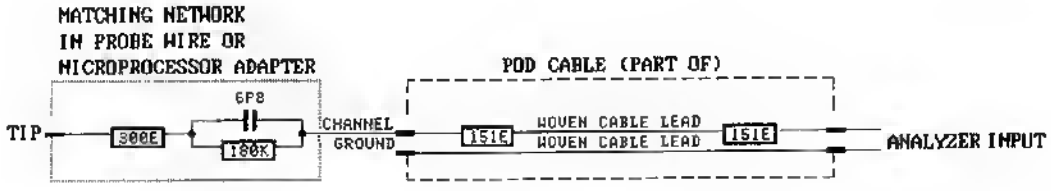


Fig. 5.1. Overall signal path.

NOTE: Only the signal wires are provided with the 151Ω matching impedance resistors.

5.2. SERVICING THE ADAPTORS.

Three models of adaptors are available:

DIP ADAPTORS DIP stands for Dual In line Package.

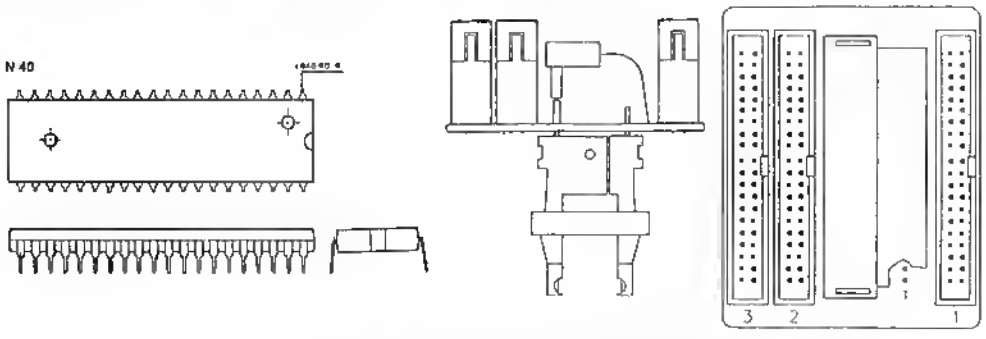


Fig. 5.2. DIP package and adaptor.

PLCC ADAPTORS PLCC stands for Plastic Leaded Chip Carrier.

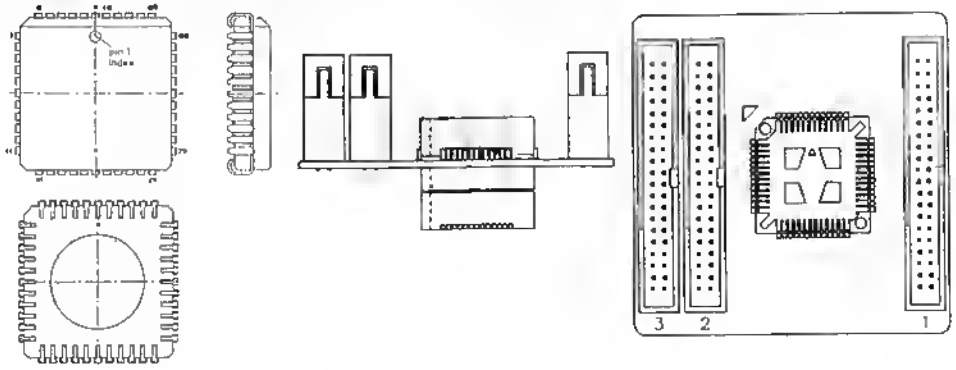


Fig. 5.3. PLCC package and adaptor.

PGA ADAPTORS PGA stands for Pin Grid Array.

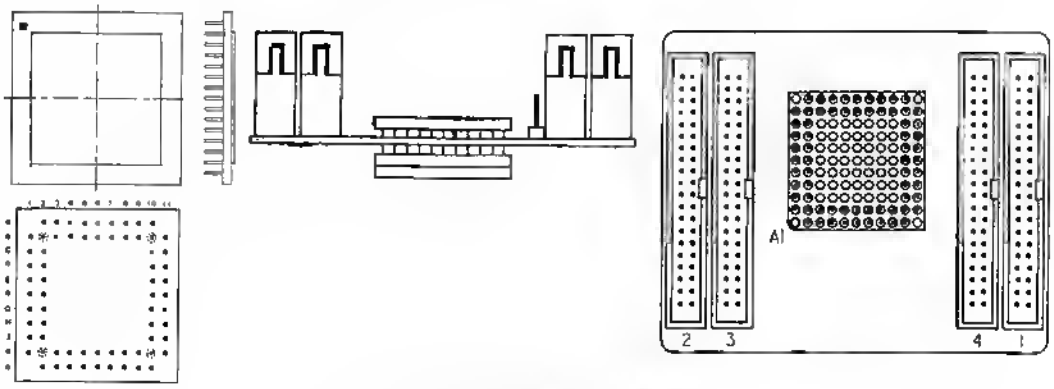


Fig. 5.4. PGA package and adaptor.

Besides the three different models of adaptors there are two types of adaptors

Passive Adaptors.

In these adaptors there are no active components involved.
They consist out of a DIP, PLCC or PGA nozzle, a PCB to route the microprocessor signals to a connector channel and the matching network for each signal channel, implemented in the adaptor connectors.
If something is wrong with an adaptor, you can check the Ohmic path from the microprocessor nozzle to the end of the woven cable.
The only things you can replace are the adaptor connectors (with the matching networks) and the woven cable.

* The adaptor connectors are available as PF 8603/20 in a set of 10.
* The woven cable is available as PF 8600/21.

Active Adaptors.

In these adaptors very specific component are used.
Except for the pod connector with the matching network nothing in these adaptors can be checked and replaced.

NOTE 1: The hardware of every adaptor is available as a repairable item (via G2). See also Chapter 9 Spare parts, section 7 Adaptors.

NOTE 2: All pinning information (from the microprocessor to a Logic Analyzer channel) of an adaptor can be found in its microprocessor support document.

5.3. CURRENTLY SUPPORTED ADAPTORS.

PF 8600/20	16CH	LOGIC POD FOR PM 358x INCLUSIVE STICKERS AND ID RINGS
PF 8600/21	16CH	POD CABLE FOR PM 358x
PF 8600/22	16CH	PROBE SET FOR PF 8600/20
PF 8600/23	16CH	LOGIC POD FOR PM 358x EXCLUSIVE STICKERS AND ID RINGS
PF 8600/24	40	MINI-MEASURING CLIPS (GREY, LOW-PROFILE)
PF 8603/20	16CH	R.C. COMPENSATED CONNECTORS (SET OF 10) FOR PM 358x
PF 8610/30	8085	DIP-CLIP PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8611/30	6800	DIP-CLIP PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8612/30	6809	DIP-CLIP PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8613/30	6502	DIP-CLIP PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8614/30	Z80	DIP-CLIP PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8615/30	8051	DIP-CLIP PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8615/32	8031/51	PLCC PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8615/82	8031/51	PLCC 15 mm EXTENSION SOCKET
PF 8616/32	68HC11	PLCC PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8616/82	68HC11	PLCC 15 mm EXTENSION SOCKET
PF 8617/32	64180	PLCC PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8617/82	64180	PLCC 15 mm EXTENSION SOCKET
PF 8618/32	80515/35	PLCC PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8618/82	80515/35	PLCC 15 mm EXTENSION SOCKET
PF 8619/32	68HC11F	PLCC PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8619/82	68HC11F	PLCC 15 mm EXTENSION SOCKET

PF 8620/30	68000/10	DIP-CLIP PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8620/31	68000/10	DIP-SOCKET PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8620/32	68000/10	PLCC PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8620/33	68000/10	PGA PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8620/81	68000/10	DIP 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8620/82	68000/10	PLCC 15 mm EXTENSION SOCKET
PF 8620/83	68000/10	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8621/33	68302	PGA PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8621/83	68302	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8622/32	68070	PLCC PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8622/82	68070	PLCC 15 mm EXTENSION SOCKET
PF 8624/30	8086/88	DIP-CLIP PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8625/32	80186/88	PLCC PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8625/33	80186/188	PGA PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8625/82	80186/88	PLCC 15 mm EXTENSION SOCKET
PF 8625/83	80186/188	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8626/32	80286	PLCC PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8826/33	80286	PGA PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8626/82	80286	PLCC 15 mm EXTENSION SOCKET
PF 8626/83	80286	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8627/32	80186/88-EB	PLCC PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8627/82	80186/88-EB	PLCC 15 mm EXTENSION SOCKET
PF 8628/32	MCS-96	PLCC PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8628/82	MCS-96	PLCC 15 mm EXTENSION SOCKET

PF 8630/33	68020	PGA PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8630/83	68020	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8631/33	68030	PGA PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8631/83	68030	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8632/33	68040	PGA PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8632/83	68040	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8634/23	386DX	PGA PERSONALITY ADAPTOR TIMING FOR PM 358x
PF 8635/33	386DX	PGA PERSONALITY ADAPTOR STATE + DISA SOFTWARE FOR PM 358x
PF 8635/83	386DX	PGA 4 mm EXTENSION SOCKETS (SET OF 3) 8x
PF 8636/23	80486	PGA PERSONALITY ADAPTOR TIMING FOR PM 358x
PF 8637/33	80486	PGA PERSONALITY ADAPTOR STATE + DISA SOFTWARE FOR PM 358x
PF 8637/83	80486	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8644/23	80960CA	PGA PERSONALITY ADAPTOR TIMING FOR PM 3585
PF 8645/33	80960CA	PGA PERSONALITY ADAPTOR STATE + DISA SOFTWARE FOR PM 3585
PF 8645/83	80960CA	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8647/33	AMD-29030	PGA PERSONALITY ADAPTOR STATE + DISA SOFTWARE FOR PM 358x
PF 8647/83	AMD-29030	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8670/32	TMS 32020/C2x	PLCC PERSONALITY ADAPTOR STATE + DISA SOFTWARE FOR PM 358x
PF 8670/33	TMS 32020/C2x	PGA PERSONALITY ADAPTOR STATE + DISA SOFTWARE FOR PM 358x
PF 8670/82	TMS 32020/C2x	PLCC 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8670/83	TMS 32020/C2x	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8671/33	TMS 320C3x	PGA PERSONALITY ADAPTOR STATE + DISA SOFTWARE FOR PM 358x
PF 8671/83	TMS 320C3x	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8675/33	DSP56001	PGA PERSONALITY ADAPTOR STATE + DISA SOFTWARE FOR PM 358x
PF 8675/83	DSP56001	PGA 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8680/36	IEEE-488	BUS ADAPTOR + DISA SOFTWARE FOR PM 358x

PF 8711/30	68008	DIP-CLIP PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8711/32	68008	PLCC PERSONALITY ADAPTOR STATE + DISA SOFTWARE FOR PM 358x
PF 8711/82	68008	PLCC 4 mm EXTENSION SOCKETS (SET OF 3)
PF 8720/34	68331/2	POFP-CLIP PERSONALITY ADAPTOR + DISA SOFTWARE FOR PM 358x
PF 8720/36	68331/2	20-PIN CONNECTOR SET + DISA SOFTWARE FOR PM 358x
PF 8724/24	i386-SX	POFP-CLIP PERSONALITY ADAPTOR TIMING FOR PM 358x
PF 8724/25	i386-SX	POFP-SOCKET PERSONALITY ADAPTOR TIMING FOR PM 358x
PF 8725/34	i386-SX	POFP-CLIP PERSONALITY ADAPTOR STATE + DISA SOFTWARE FOR PM 358x
PF 8725/35	i386-SX	POFP-SOCKET PERSONALITY ADAPTOR STATE + DISA SOFTWARE FOR PM 358x

For spare parts please refer to chapter 9.

NOTES:

CHAPTER 6.

6. DIAGNOSTIC TESTS.

CONTENTS.

6.1 GENERAL INFORMATION.

Diagnostic tests are Intended to be used for the acceptance inspection of new instruments or for diagnostic purposes.

It is not necessary to remove any of the Instrument covers as all tests are performed internally. There are three types of tests available.

1. The ***Power On Self Test*** **(POST).**
   Tests the CPU part automatically.
   This test can be done without any additional test equipment and is invocable by customers to perform diagnostic field tests.
   All basic functions of the CPU part will be tested like RAM/ROM memory as well as floppy controller,floppy drive and the Multi-Functional Peripheral.
   The test is self running and invoked by a depressed key during power on of the instrument.
   After finishing the test, the instrument continues with a normal boot of the main software.

2. The ***Diagnostic Test on floppy***.
   Manually test of CPU part.
   This test is a more extended test then the POST and requires some extra test connectors.
   This self boot-able test floppy is normally used in the service workshop and not intended for customers.
   It also contains life tests to be used during long term measurements.

3. The ***Boundary Scan Test***.
   Tests analyzer part only.
   The Boundary Test software is intended for the analyzer part only. To be able to run this test, as well as to display the test results, the CPU part must be 100% in order.
   The BST floppy "PM 358x BST PROGRAM" is self boot-able while for the various main board types different "BST Vectors" floppies are available.

NOTE: If a failure exist in the CPU ram area where a test program is loaded into, then the above mentioned tests may lock up the instrument.

6.1.1 TEST EQUIPMENT.

The peripheral equipment required during the diagnostic tests loaded from floppy is listed below.

	Service code
RS-232-C Loop-back test connector	5322 693 91418
Centronics diode matrix connector	5322 693 91479
Logic target (Commercial Item)	PF 8669/20
Extension cable for the VDU	5322 321 61069
Extension cable for the keyboard	5322 321 61068
PM 358X BST & Diagnostic test disks	5322 310 10493

The ***extension cables*** mentioned are intended to use when the main board is maintained outside the main cabinet.

6.2 POWER ON SELF TEST (POST).

6.2.1 GENERAL.

The Logic Analyzer can perform a comprehensive performance and diagnostic test at power-on. This self test procedure is performed for the CPU part of the main board and invoked if any one of the keys on the keyboard was pressed when the instrument is switched on.
When the POST is invoked the release and software versions of the internal main board EPROM's and the keyboard EPROM are displayed.
The procedure calculates the Check-sum of the EPROM's, tests the operation of the RAM, checks the status of the disk controller and the interrupt of the MFP. If an error is detected the procedure will be terminated and the failure report displayed on the screen.
If no errors are found a normal boot of the main software is invoked automatically.

NOTE: Refer to the section "DIAGNOSTIC TEST DISKETTE" for explanation of error messages during the POST.

6.2.2 STACK TEST.

The static RAM area should be tested first, before any test can be performed. The area is used as stack area for the various tests to come.
If a failure occurs in this part of the POST, no further testing is possible before the failure is cleared.

6.2.3 ROM TEST.

On the main board two EPROM's contain the resident cold-start boot software. One EPROM contains the even addressed data bytes while the other contains the odd addressed data bytes. This test calculates the Check-sums of the EPROM's. Information will only be displayed in the case of an error and will include the Check-sum calculated and the Check-sum that has been read from EPROM.
The even EPROM is D400 and the EPROM indicated as odd is D403.

6.2.4 RAM TEST.

This test checks the correct operation of the dynamic RAM and the static RAM. Information containing the current address being tested will be displayed. If an error is found during the test procedure an error message will be displayed and the test will stop. For more information about the address ranges see the table of Chapter 6.3.1.

NOTE: Testing the complete RAM area, will take approx 6 minutes.

6.2.5 FLOPPY CONTROLLER TEST.

This test checks the disk controller chip and the ready status of the drive.
Also a drive select is performed.
If an error is found an error message will be displayed and the test will stop.

6.2.6 MULTI FUNCTION PERIPHERAL (MFP).

This test starts the counter of the MFP and waits for an interrupt from the counter. If an interrupt is not received then an error message is displayed stating that the MFP is inoperable.

6.3 DIAGNOSTIC TEST DISKETTE.

Besides a Power On Self Test which is resident in EPROM a more intensive testing can be achieved by the diagnostic diskette software. A big difference in comparison with the POST is the fact that the floppy must be able to be loaded and run by the CPU section, if not, only the POST can be used to perform the diagnostics.

The description of the 1.0 version of the PM 358x DIAGNOSTIC (Type Number 5322 310 10493) is given in this Chapter.

order
898668

On this self boot-able diskette a lot of individually invocable tests are available. However, some of the tests require the use of extra hardware to be connected, for example the RS-232 loop-back connector and the centronics parallel connector.

In order to gain access to the selectable tests on this floppy it is necessary to perform the following procedure:

1. Power OFF the instrument.
2. Insert the "PM 358x DIAGNOSTIC" disk.
3. Power ON the instrument, the test selection menu will now appear.

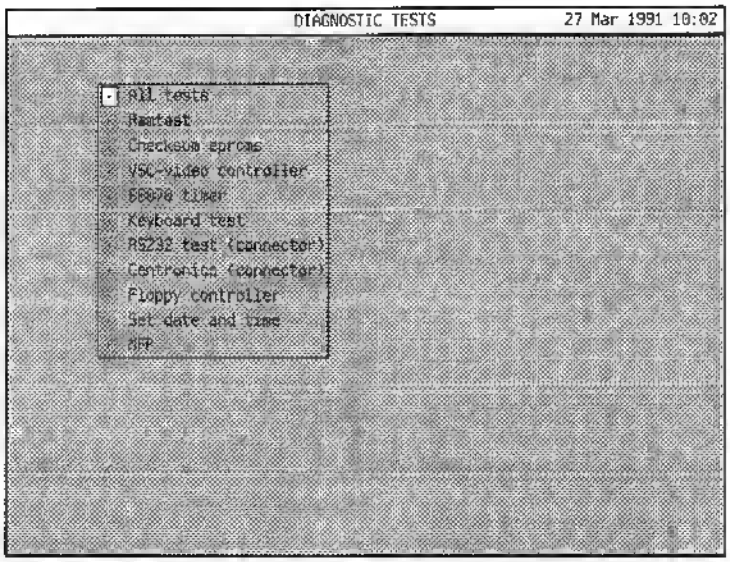


Fig. 6.1. Test selection menu.

To select a test, dial the cursor to the box indicating the test desired and then press SELECT.

NOTE: **All tests** is not implemented in release 1.0.

A menu will then appear showing the test to be performed and a brief description. The test will commence when the cursor has been moved to the type of test required and "RUN" is pressed.

To leave a test the cursor should be moved to the box containing an "X" (no change) or "V" (confirmation) on the title line by means of the up arrow key and pressing SELECT.

In many of the menu's there are modes to be set like "Single test", "Stop on Error" and "Repetitive test". The mode is selected by moving the cursor to the required option before "RUN" is depressed.

6.3.1 RAM TEST.

This test checks the proper operation of the RAM.
The addresses tested are:

1C0000 - 1DFFFF (stack) Static Ram
000000 - 17FFFF (system) Dynamic Ram

If an error is detected and the mode of testing is "Stop at error" then the system starts looping at the faulty address.
In this mode conventional equipment can be used to trace read and write cycles and address data latch accesses at that particular memory position to locate the faulty component.

NOTE: The Dynamic Ram memory is controlled by the Video System Controller (IC D105). It should be noted that for the Dynamic Ram memory the faulty address indicated on the screen is shifted one address bit to the left compared to the real 68070 address. This means that ADR01 of the 68070 is MA00 of the DRAM memory. Example: If the test announces on the screen an open address line at address 1008 (i.e ADR03 of the 68070) then line MA02 to the DRAM is open !!

The diagnostic test program shows you the address where the error occurred as well as the data read compared to the written data to that address. The name of the faulty RAM IC is found by analyzing the fault reported.
Because of the use of dynamic RAM's with a 4 bits data width, the data nibble involved is of importance.
The following table might be of great help when the fault is in a RAM chip itself.
This table filters out the suspected chip.

FAILURE IN RANGE 000000 - 07FFFF:

	Low data nibble	High data nibble
Fault in even address	D1004	D1005
Fault in odd address	D1000	D1001

FAILURE IN RANGE 080000 - 0FFFFF:

	Low data nibble	High data nibble
Fault in even address	D1006	D1007
Fault in odd address	D1002	D1003

FAILURE IN RANGE 100000 - 17FFFF:

	Low data nibble	High data nibble
Fault in even address	D1022	D1023
Fault in odd address	D1020	D1021

FAILURE IN RANGE 1C0000 - 1DFFFF
The static RAM's are oriented byte-wise per address so:

	Odd address	Even address
Fault in range 1C0000 - 1CFFFF	D402	D401
Fault in range 1D0000 - 1DFFFF	D405	D404

Information displayed during a "repetitive test" includes the number of tests completed so far and the number of failures it has found.

The test can be stopped at any time by pressing the "STOP" button. The 4K block being tested at that moment will be completed before the test will stop.

6.3.2 CHECK-SUM EPROM's.

This test calculates the check-sum of the EPROM's and compares the result to that of the pre-programmed check-sum located in the EPROM's.

The options that can be selected are Single test, Stop on Error and Repetitive test. The information displayed after each test is:

- If faulty, the calculated check-sum is displayed.
- If correct the text "OK" is displayed.

If an option other than single test has been selected then the test cycle can be stopped by pressing the STOP key on the integral keyboard. Note that the test cycle in progress will be completed before you can exit Check-sum, but the time to complete this test cycle is negligible.

Faults can be located in IC D400 and D403. D400 contains the even address bytes and D403 contains the odd address bytes.

6.3.3 VIDEO CONTROLLER TEST (VSC).

When this test is selected a four-level grey-scale will appear on the screen. The scale takes the form of 34 x 31 boxes, with a boundary of squares containing four dots to be used as reference when an adjustment is made to the focusing. The display should also be central on the screen, this can be detected by referring to the small grey box in the exact centre of the display.

Furthermore the ***video alignment*** can be performed for:
- setting the correct linearity, horizontal and vertical.
- setting the correct height and width.
- setting the barrel/pincushion correction.

The display is continuously written to the screen so that the video signals are continuously measurable by conventional equipment from source to picture tube.

The test can be exited by pressing the select switch, in the case of this test the select switch acts in toggle mode.

For adjustment of the monitor settings refer to Chapter 4, Section 2: Adjustment Procedures.

6.3.4 68070 TIMER TEST.

The internal interrupt mechanism of the CPU's timers is tested.
If this test is correct the message on the screen is:

"Timer function 68070 : OK"

If this test is NOT correct the message on the screen is:

"Timer function 68070 : NOT OK"

In this case the 68070 internal timer is bad and the complete 68070 chip (D102) must be replaced.

6.3.5 KEYBOARD TEST.

When the Keyboard test has been selected a representation of the keyboard lay-out is displayed on the screen. When a key is pressed the corresponding key will be highlighted on the screen. If the dial is rotated the two boxes in the lower centre of the screen highlight. The direction of rotation of the dial is indicated with arrows.

The exception to this is the PRINT key, when this is pressed the print menu is displayed, this in itself verifying the correct operation of the key.

If any of the keys, with the exception of PRINT, is pressed three times in succession then the keyboard test is concluded and you are returned to the test selection menu.

To test the SHIFT key on the keyboard you must also press a letter, this will then highlight the SHIFT and the letter key on the screen.

6.3.6 RS-232 CONNECTOR.

In order to complete this test a specially adapted 25 pole
D-type plug (see chapter 9.8 "Spare Parts") must be used.
The plug must be inserted in the serial output socket on the rear of the instrument.
The connections on this plug are:

Pin 2 (TXD) to Pin 3 (RXD)
Pin 4 (RTS) to Pin 5 (CTS)

This connector enables the Transmit-Receive loop-back to be tested.

The diagnostic test performs 2 serial tests successively.

- The local internal transmit- receive loop is tested in the 68070 itself.
  A software short internally in the CPU is achieved.
- The external loop-back is tested via the loop-back connector.

Test characters are transmitted as follows:

First, the Request to Send (RTS) output is made active. Because of the interconnection between the RTS and the Clear to Send (CTS) the transmission of the test character is enabled and the CPU transmits the character via the TXD output. Due to a similar interconnection between the TXD and the RXD the same character is received and can be analyzed for correctness.
If nothing is received, the message will be:
receive error: sent data xx
If wrong data is received, the message will be:
receive data: yy sent data: xx
Where xx is the actual character sent, ranging from H"00" to H"7F", and yy is the actual received data.

6.3.7 CENTRONICS TEST.

The centronics test checks each output pin connection. In order to complete this test the following specially adapted 25 pole D-type plug (see chapter 9.8 "Spare Parts") must be connected to the centronics output on the rear of the instrument.

Connections must be made as shown in Fig. 6.2.
Note that there are no connections on pins 14 to 25 inclusive.

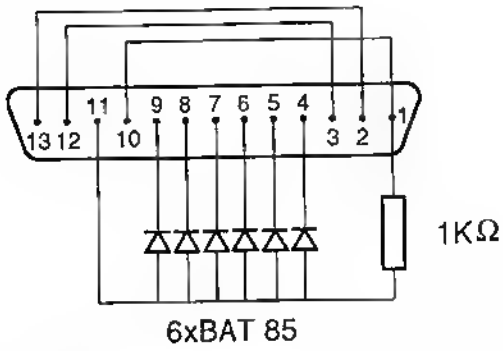


Fig. 6.2. Centronics diode matrix connector.

The signals on the pins are as follows:

1	STROBE	8	data 6
2	data 0	9	data 7
3	data 1	10	ACKNOWLEDGE
4	data 2	11	BUSY
5	data 3	12	PAPER END
6	data 4	13	SELECT
7	data 5		

Before the test signals are sent to the parallel output connector the internal loop-back in the PPI is tested. An error in this path will say "PPI failure (D701)" and the test will stop. If the PPI functions correctly, nothing is displayed, and the test will continue. The path from the PPI, via the output buffers, to the output connector is activated in the following way.

1) A strobe pulse is sent to pin 1 (STROBE) and a check is made on pin 10 (ACKNOWLEDGE) for the same pulse.
2) Data 0 is pulsed and checked via pin 13 (SELECT)
3) Data 1 is pulsed and checked via pin 12 (PAPER END)
4) Data 2 to Data 7 are pulsed individually and read back via the same pin 11 (BUSY)

If an error is detected, in item 1, 2, 3 or 4, the failed line is announced in the error report. If, however, in item 4 the BUSY line is broken data 2 to data 7 will be announced as faulty. This is because BUSY is involved in all the tests from data 2 to data 7 due to the design of the test plug.

NOTE: A short circuit between data lines 3 until 7 can not be detected in this test.

As with other tests the test mode can be set to Single, Stop on Error or Repetitive.

6.3.8 FLOPPY CONTROLLER.

When this test is invoked a message pops up to use a scratch diskette since there are read and write actions performed during this test.
To start the test press "RUN".
The following items will be tested in the given order:

a) The disk change signal from the drive to the CPU. This signal will be toggled whenever a disk is exchanged.

b) FDC initialization
This program tests the ability to initialize the floppy disk controller chip on the main board.

c) Selection of the drive
By selecting and deselecting the drive the drive select LED on the front of the analyzer will blink. The blinking indicates the correct selection of the drive.

d) Opening Floppy Device
This is a software procedure to open the floppy device driver for floppy access actions. First the write protect flip-flop in the drive is tested, controlled by the opto-electronic sensor in the floppy drive.
If the device is open for a write action whilst the floppy is write protected, the opening of the device driver will fail.

e) Clearing track 76
The track must be cleared (with pattern 00) before the test starts to remove any information that has been written to it during a previous test.

f) Reading track 76
Reads the cleared track.

g) Writing track 76
A binary pattern is written on this track (0-255 Hex) in order to test the write quality of the drive. This information is used in the next test. If writing fails (i.e. no track access) an error will be displayed.

h) Reading track 76
The previously written information on track 78 is scanned and a verify is done on bad data, CRC errors etc.

i) Closing Floppy device
This tests the ability to close the software driver after the previous tests. If the floppy issues a not ready status the test will be faulty.

6.3.9 SET DATE AND TIME.

This option allows the alteration of the system clock with regard to date and time and the format of presentation.

You can choose the time format required by moving the cursor to the appropriate box and pressing the "SELECT" button.
The format is changed immediately while the time must be verified before exiting.

To exit this menu move the cursor, using the arrow keys, to highlight either of the boxes on the test title line, and press SELECT. If the box on the left is highlighted on leaving the test the new time is validated. If the box on the right is highlighted the new time will not be validated.

6.3.10 MULTI-FUNCTION PERIPHERAL (MFP).

The Multi-Function Peripheral test tests the interrupt of timer A from this chip on edge triggered and level triggered values.

6.3.11 LOGIC TARGET.

The logic target PF 8669/20 can be used to generate a binary count data pattern. The ripple counter in this logic target directly outputs its counter value to the channels 0 - 11 of the analyzer (Outputs o1 - o12 of the logic target). Channel 12 and 13 carry the inverse signals of channel 0 and 1 respectively. If the mode switch is set to MODE I, channel 14 will carry a negative going glitch of approx. 4 ns and channel 15 will carry the counter clock signal. In MODE II channel 14 and 15 carry respectively the inverse signal of channel 2 and 3. The Logic target can be set to either 2 MHz or 15 MHz by means of the switch CLOCK FREQ.
The analyzer supplies the +5V operating voltage for the counter via the POD cable.

6.4 BOUNDARY SCAN TEST.

6.4.1 GENERAL INFORMATION.

In this chapter it is assumed that the user is familiar with principles of Boundary Scan Test techniques.
The Boundary Scan test is used to test the main-board's analyzer section. It can perform a low speed static internal ASIC test as well as a check on all interconnections between the various ASIC pins soldered on the board. A test architecture was developed encompassing software tools and data formats that are required for test pattern generation, test engineering, test execution and diagnostics.

The explanation below is for VERSION 1.0 of Type Number 5322 310 10493 BST.

NOTE: The BST test program must be run without any input signal coupled to the POD inputs.

The available floppies for the various analyzer types are:

ANALYZER TYPE	BST FLOPPY
All versions	PM 358x BST Program
200 MHz 96 channels	PM 3585/90 BST Vectors part 1 and part 2.
200 MHz 64 channels	PM 3585/60 BST Vectors part 1 and part 2.
100 MHz 64 channels	PM 3580/60 BST Vectors part 1
100 MHz 32 channels	PM 3580/30 BST Vectors part 1

NOTE: For Service Code numbers refer to chapter "SPARES".

The boot-able floppy "BST Program" must be used with any analyzer type to start the boundary scan diagnostics.
When the BST Program has booted the "BST Vectors" floppy can be inserted in the drive.
After pressing "SELECT" the "BST Vectors" floppy is read by the drive and a survey of test files available on that floppy is shown on a menu.

NOTE: The Boundary Scan tests can only run when the analyzer CPU part is operative, allowing the BST software to be loaded via the floppy drive.

As an example only the 200 MHz 96 channel test software will be explained.
The test software for the other types of analyzers is a subset of this function.

The following tests can be found on the 200 MHz 96 Channel BST Vectors part 1 diskette.

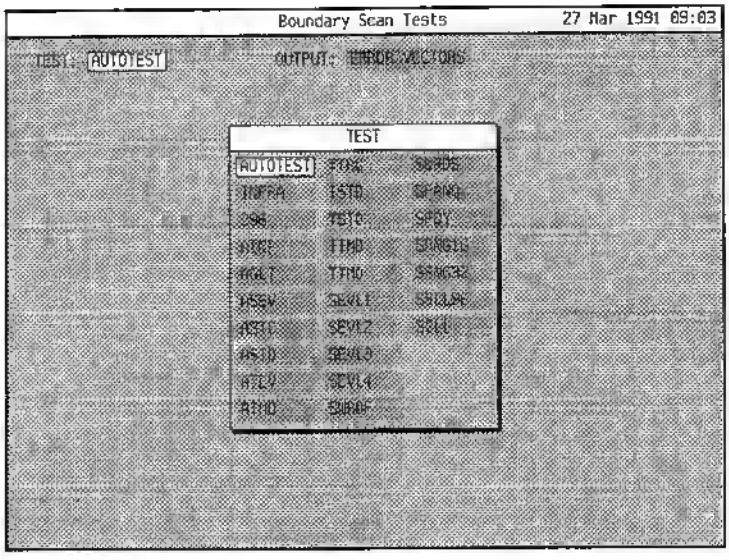


Fig. 6.3. Boundary Scan test disk 1.

A second diskette BST Vectors part 2, is required to complete a functionality test on the Acquisition and Time ASIC's.

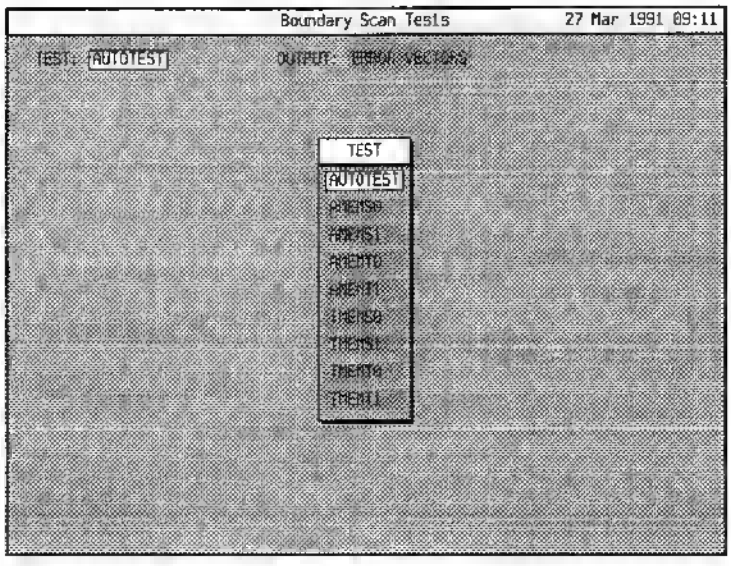


Fig. 6.4. Boundary Scan Tests disk 2.

NOTE: The PM 3580 BST floppy contains the sum of the PM 3585 BST floppy's 1 and 2.

Note that the first character of the test name signifies the type of ASIC involved in that test.

A = Acquisition ASIC's.
T = Time ASIC's.
S = Sequencer ASIC's.

BST vectors part 1 of 2

AUTOTEST	Runs all tests automatically.
INFRA	Tests the BST chains infrastructure.
296	Tests all interconnections between ASIC's.
AINP	Testing inputs through the input ASIC's.
AGLT	Data storage glitch mode.
ASEV	Acquisition state events.
ASTC	Clock storage state mode.
ASTD	Data storage state mode.
ATEV	Timing events.
ATMD	Data storage in timing mode.
TTRG	Combination of trigger events.
TSTD	Data storage in state mode.
TST0	Counter overflow in state mode.
TTMD	Data storage in timing mode.
TTMO	Counter overflow in timing mode.
SEVL1	Event logic event 1.
SEVL2	Event logic event 2.
SEVL3	Event logic event 3.
SEVL4	Event logic event 4.
SWRDF	Trigger of final word.
SWRDS	Trigger of slow words.
SFANQ	Time words and qualifiers.
SFDY	Final delay.
SRNG16	Range logic 16 bit.
SRNG32	Range logic 32 bit.
SSLL96	Level changes.
SCLL	Counter cells.

BST vectors part 2 of 2

AMEMS0	Memory test State with 0
AMEMS1	Memory test State with 1
AMEMT0	Memory test Timing with 0
AMEMT1	Memory test Timing with 1
TMEMS0	Memory test State with 0
TMEMS1	Memory test State with 1
TMEMT0	Memory test Timing with 0
TMEMT1	Memory test Timing with 1

NOTE 1: The numbers **296, SSCL96** denotes that the test is for the 200 MHz 96 channel model, **132** and **SSCL32** are intended for the 100 MHz 32 channel model, etc.

NOTE 2: If the **INFRA** test fails then there is no BST possible and hence the interconnect test will fail on all possible bit-cells resulting in a very long error report.

Test **296** checks the correctness of interconnections between all ASIC's and on permanent "0" or "1" levels when ASIC pins are stuck to ground or +5V. Also bridging faults between solder tracks and position stuck at faults are traced.

NOTE: Interconnect tests like **296**, **264**, **164** and **132** can fail sometimes due to timing tolerances, however if this test passes once, the hardware interconnections will be correct.
There is a method to analyze the result of this interconnection test when by mistake the test fails.
When the output is set to "error vectors", the used test-pattern is shown in the first column, and the BST cell-number in the third column of the error report. These 2 columns should be checked carefully to detect a possible mistaken error announcement.
If in each error line the test pattern is equal while the cell numbers are random numbers then do start a new test, because there might be no errors. If however the test-pattern numbers differ and the bit-cell numbers are equal then there is a real fault. The "pinning" report will give more detailed information where the fault is situated.

6.4.2 ERROR REPORTS.

The following test types can be executed:

- Interconnection test which tests the interconnection between the ASIC's. (test 296, 264, 164 and 132)

- Functional/Specification tests.
  This is a low speed Internal ASIC test.

After a test is selected with the dial, followed by the "SELECT" button, the "TESTNAME" is copied into the box "TEST:".

The test result or error report output can be selected to 4 different modes i.e: ERROR VECTORS, PROBABILITY, PINNING or DIAGNOSTIC information.
By moving the cursor into the box "OUTPUT:" and pressing SELECT a pop-up window is shown.
After pressing RUN the test is loaded and started automatical.
The result of the test is displayed according to the setting of box "OUTPUT:". This setting can be altered to other modes after each test to obtain the desired error output information (only modes making sense are selectable).

ERROR VECTORS, PROBABILITY and PINNING reports have no meaning with functionality tests and hence the output will always be displayed as DIAGNOSTIC (faulty ASIC name and ASIC IC-number).

6.4.3 ERROR DEFINITIONS.

ERROR VECTORS: Necessary information for software conversion programs to assign located faults to pin numbers of ASIC's. These error vectors are of no interest to the user.

PROBABILITY: Because of the complexity and variety of connections between the ASIC's a "stuck to "0" line" can be caused, for example, by all the ASIC's which are connected to that "stuck to "0" line". The BST software will indicate the probability that the ASIC that has been mentioned as faulty is actually the cause.

PINNING: The result of the diagnosis (table of error vectors) is converted to the pin numbers of ASIC's. The fault can be differentiated as a stuck to "1" or "0" or as a bridging or as a position stuck-at problem.

DIAGNOSTIC Via software the error vectors are interpreted to show as a final result the faulty IC and IC number.

6.4.4. EXPLANATIONS OF ERROR REPORTS.

6.4.4.1 Error report ERROR VECTORS.

Example of a stuck to "0" shown as ERROR VECTORS:

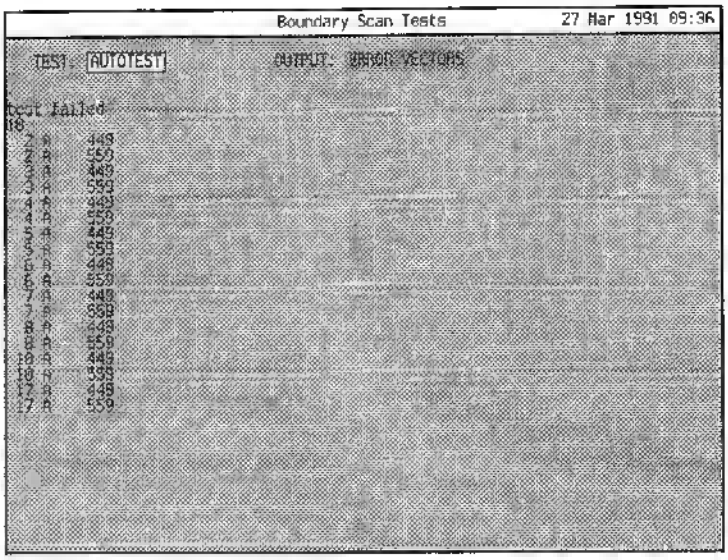


Fig. 6.5. Error message with VECTORS.

The survey shows that the selected test file "AUTOTEST" was faulty. In fact AUTOTEST is the total collection of tests available and one failed.
There are in total 18 vectors displayed of faults detected in the various nets.
The line " **2 A 449** " means:

2 = The fault was detected using test-pattern 2.
A = The faulty chain name is "A".
449 = Element number 449 of shift registers was involved.

For the user the vectors are of no use to find the fault.
These vectors are used for the translation software to create the pinning and probability reports, explained on the following pages.

6.4.4.2 Error report PROBABILITY.

The error report of a certain fault can be display in PROBABILITY.
The chance that a fault located is caused by a suspected component (in percentage of certainty) is called PROBABILITY.
A PROBABILITY error report might look like:

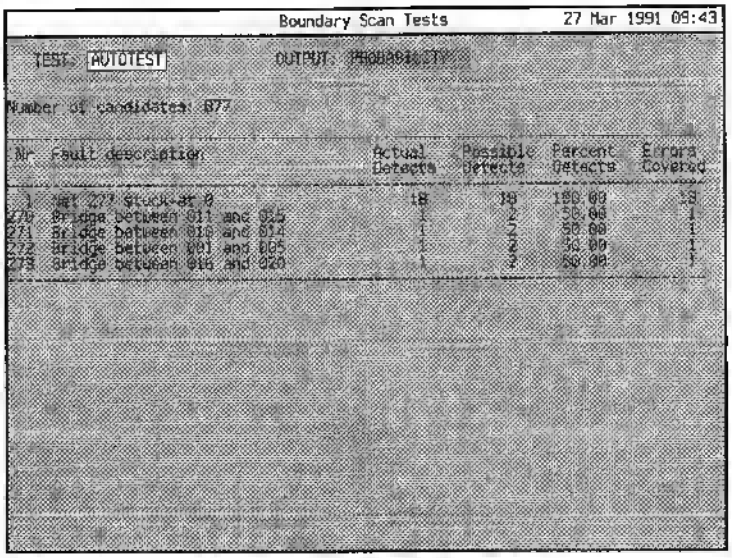


Fig. 6.6. Error report PROBABILITY.

The error reports items are explained below i.e.

Number of candidates: There are found 877 faulty bits in the total sensed serial bit-stream. Out of these candidates the nets involved are calculated as well as the type of error in or between mutual nets

Nr: The number of the net involved.

Fault description: The fault can be shown as "stuck at 0/1" in a net or "bridging" errors between the various nets.

NOTE: A "stuck at" error can cause in other nets bridging faults with less coverage percentage.

Actual Detects: The number of failures actually detected during testing.

Possible Detects: There are 18 patterns to detect a stuck to "0" in Net 277 (18 possible detects).

Percent Detects During analyses of the error result by the software all 18 patterns indeed did contain a stuck at "0" somewhere in the chain corresponding to Net 277 (18 actual detects).
This means a coverage of 100%.

Errors Covered All 18 errors were covered in the error report.

NOTE: The probability error report is given in terms of the faulty net, and not as the ASIC pin number. The pinning report explained on the following pages is of greatest interest to the Service technician.

6.4.4.3 Error report PINNING.

The result of a faulty test can be converted into involved pins of ASIC's. The error report PINNING can only be sensed by interconnection tests (296, 264, 164 and 132). The information displayed can be pin numbers of ASIC's which are stuck at "0" or stuck at "1". Also pins which are interconnected by solder (Net bridging faults) or badly soldered pins (Position stuck-at faults) can be found.
An example of a stuck at fault displayed in PINNING mode can be:

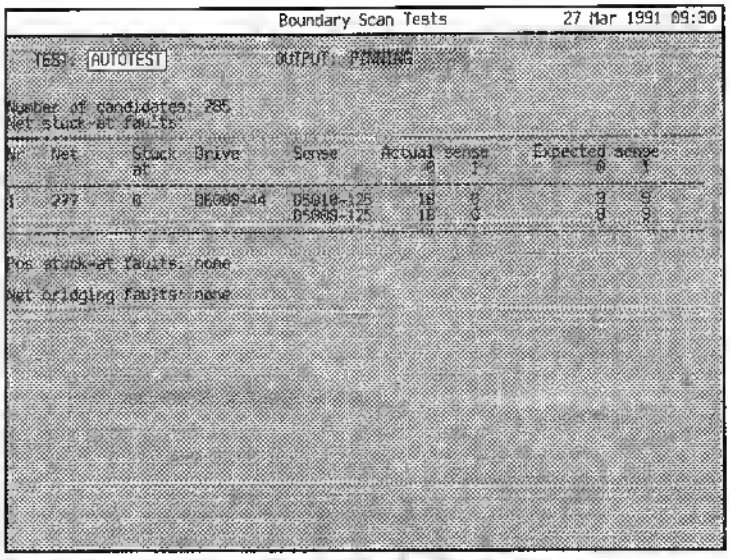


Fig. 6.7. Stuck at error report with PINNING.

Number of candidates See error report Probabilities.

Nr	Map number, this is a consecutive number.
Net	The number of the faulty net.
Stuck at	Type of error.
Drive	Sending IC and pin number.
Sense	Receiving IC's and pin numbers.
Actual sense	The number of "0"'s and "1"'s found after toggling the net.
Expected Sense	The number of "0"'s and "1"'s when the net was OK.

This error caused a detection in Net number 277 and the type of error was "stuck at 0".
The fault was detected by toggling the signal of D6000 pin 44 (Drive) and looking to pins 125 of both D5010 and D5009 (Sense).
Pin 44 of D6000 is connected via a print-track to pin 125 of D5010 and to pin 125 of D5009.

When this track was set to "1" 9 times with drive cell D6000-44,then a "0" was sensed 9 times at pins 125 of D5010 and D5009. Also when the Drive was set to "0" 9 times there was sensed 9 times a "0".

The software however expected when everything would be correct 9 times to sense a "0" and 9 times to sense a "1" on both the sense pins (D5010-125 and D5009-125) however there was sensed 18 times a "0". Conclusion: The net between D6000-44 and both D5010-125, D5009-125 is shorted to ground.(Stuck at "0").

At a bridging error the PINNING error report is more complex compared to "stuck at" error reports. An example of such a report is explained below:

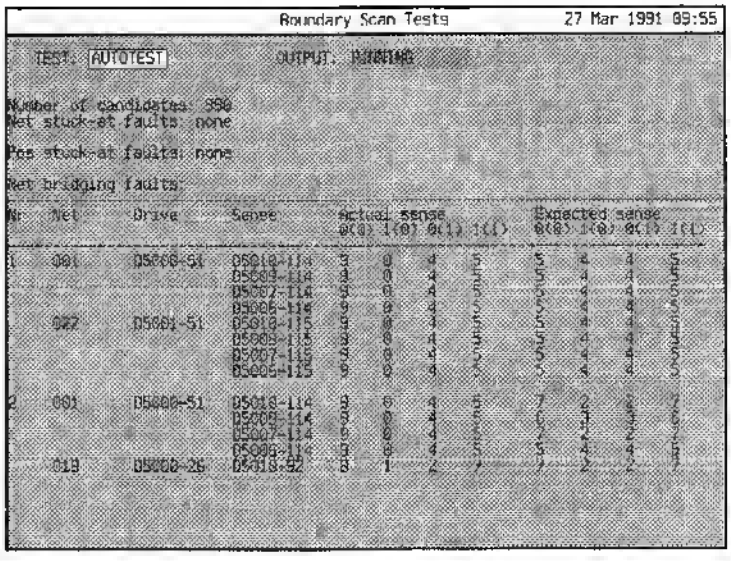


Fig. 6.8. Bridging error report with PINNING.

This error report gives a total of 990 fault candidates in the BST-chain.
There were no "Net" or "Pos(ition)" stuck-at faults detected.

The detected faults were of the type "bridging".
This means that there were shorts detected between print tracks, causing nets to be interconnected.
The error report contains several report maps but here only map 1 (see column "Nr") and part of map 2 is visible.
For understanding the report, only map 1 will be explained.

Nr	Map number ,this is a consecutive number.
Net	The number of the faulty Net.
Drive	The I.C. number and pin of the driving output in that net.
Sense	The I.C. numbers and pins of the receiving (sensing) inputs of that net.
Actual sense	The logical values sensed (found) during testing of the net.
Expected sense	The expected logical values (no error values).

There are always 2 nets involved when there are bridging errors. In this example Net 001 and 022 are involved.
Because of the fact that 2 nets are always involved and bridged, the sense input can receive also information from both drives of each net.
This is displayed in the fields "Actual sense" and "expected sense".
The 4 possible bit values of both driver cells are displayed as 0(0), 1(0), 0(1) and 1(1).
The value in brackets is that of the second net driver (in this example net 022) and the value without brackets is that of the first net driver (in this example 001).
Only this value is sensed and counted in that column.

i.e. 0(1) means: driver of first net (001) was a "0" while driver of second net (022) was a "1".
1(1) means: driver of first net (001) was a "1" while driver of second net (022) was a "1".
etc.

In map 1 there are 4 sense pins and 2 drive pins.
The first line of map 1 shows in the segment "Expected sense" for the value 1(0) 4 times to expect a 1 when D5000-51 (D5000 pin 51) drives a "1" and D5001-51 (D5001 pin 51) drives a "0".
The counted value 0 in the "Actual sense" segment for the value 1(0) shows that drive D5001-51 of net 022 is the strongest and presses a "0" on the bridged tracks.
For the value 0(1) it is just inverse, here D5001-51 is the weakest and cannot presses a "1" on the bridged tracks when D5000-51 presses a "0" on the tracks.
Conclusion:There is a bridge between D5000-51 and D5001-51
which is sensed in both nets between pins 114 an 115 of the following I.C.'s: D5006, D5007, D5009 and D5010.

6.4.4.4 Error report DIAGNOSTIC.

This error report is used mainly with the functionality test. It shows the computed result of the error vectors as the faulty IC name and number. I.e. D5001 not working correctly.

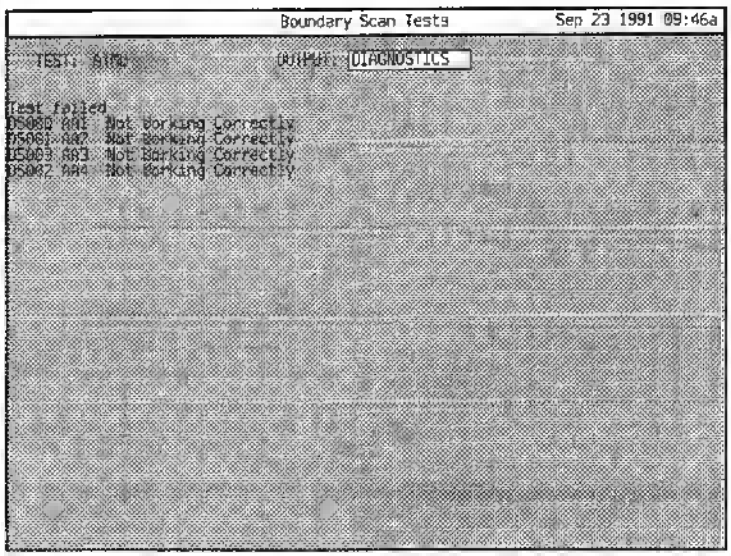


Fig. 6.9. Error report with DIAGNOSTIC.

CHAPTER 7.

7. CORRECTIVE MAINTENANCE.

CONTENTS.

7.1 REPLACEMENTS.

WARNING: THE CONNECTION BETWEEN THE EHT CABLE AND THE EHT TRANSFORMER IS UNBREAKABLE. WHEN THE EHT CABLE TO THE POST ACCELERATION ANODE IS DISCONNECTED, THE CABLE, AS WELL AS THE CRT TERMINAL, MUST BE DISCHARGED BY SHORTING THE TERMINALS TO EARTH.

7.1.1 STANDARD PARTS.

Replacements for electrical and mechanical parts can be obtained through your local Philips organization or representative. Before purchasing or ordering replacement parts, check the parts list for the value, tolerance, rating and description.

NOTE: Physical size and shape of a component may affect the operation of the instrument, particularly at high frequencies. Always use direct replacement components, unless it is known that a substitute will not degrade the instruments performance.

7.1.2 SPECIAL PARTS.

In addition to the standard electronic parts, some special components are used:

- Components, manufactured or selected by Philips to meet specific performance requirements.
- Components that are important for the safety of the instrument.

ATTENTION: Both types of components may only be replaced by components obtained through your local Philips organisation or representative.

7.1.3 TRANSISTORS AND INTEGRATED CIRCUITS.

- When a device has been replaced the operation of the part of the instrument affected must be checked.
- When re-installing power-supply transistors use silicon grease to increase the heat transfer characteristics.

WARNING: HANDLE SILICON GREASE WITH CARE. AVOID CONTACT WITH EYES AND WASH HANDS CAREFULLY AFTER USING SILICON GREASE.

7.1.4 STATIC SENSITIVE COMPONENTS.

This instrument contains electrical components that are susceptible to damage from static discharge. Servicing static-sensitive assemblies or components should only be performed at a static free work-station by qualified service personnel.

7.2 SOLDERING TECHNIQUES.

7.2.1 SEMICONDUCTORS.

Method

1. De-solder each tag of the semi-conductor individually.

2. Remove all superfluous soldering material, this can be done by using either a sucking iron or sucking litze wire.

3. Check that the tags of the replacement part are clean and pre-tinned on the soldering points.

4. Locate the replacement semi-conductor exactly, and solder each tag to the relevant printed conductor on the circuit board.

NOTE: The maximum permissable soldering time is 10 seconds, during which time the temperature of the tags must not exceed 250°C. It is recommended that you use a solder with a low melting point.

Take care not to damage the plastic encapsulation of the semiconductor, the softening point of the plastic being 150°C.

ATTENTION: When you are soldering inside the instrument it is essential to use a low-voltage soldering iron, the tip of which must be grounded to the mass of the instrument.

Suitable soldering irons are:

- ORYX micro-miniature soldering instrument, type 6A, Voltage 6V, in combination with PLATO pin-point tip 0-569.

- Low voltage mini soldering iron, type 800/12W - 6V, power 12W, voltage 6V, in combination with 1 mm pin-point tip.

Ordinary 60/40 solder with core and a 35W to 40W pencil type soldering iron can be used to accomplish the majority of the soldering. If a higher wattage rating soldering iron is used on the etched circuit boards the excessive heat can cause the etched circuit wiring to separate from the board base material.

7.2.2 MICRO-MINIATURE SEMICONDUCTORS.

Because of the small dimensions of these components and the lack of space between them when mounted on a PCB it is necessary to use a miniature soldering iron with a pin-point tip, that has a maximum diameter of 1 mm, to solder them to the PCB.

7.2.3 ASIC's.

7.2.3.1 Special tools.

In order to remove and replace the Surface mounted ASIC's the following ***soldering/de-soldering equipment*** is recommended.

- Leister-Labor <<S>> or Leister-Hot-Jet, hot air soldering/de-soldering tool, with the following nozzles:

  * 2.5 mm round nozzle and 15.4 x 9.5 rectangular nozzle.
  * PLCC 20, PLCC 28, PLCC 44, PLCC 52, PLCC 68, PLCC 84.
  * SO 20L, SO 16L, SO 16.
  * SIP 25 mm.
  * PGA 68.

- A small metallic block to act as a heat sink for the ASIC, ideally one surface of the block being the same, if not smaller, than that of the ASIC.

7.2.3.2 Method of replacing components.

NOTE 1: If You do not have the proper equipment or do not feel confident enough, repair by the supply centre is also possible.

NOTE 2: All of the ASIC's can be exchanged using the following method with the exception of the clock ASIC D6000.
For the removal of the clock ASIC refer to section: 7.2.3.3.

NOTE 3: Before replacing an ASIC, check if the old chip is provided with a heatsink, if so, mount on the new chip to be installed the heatsink fastener on ASIC with ARALDIT glue.

HEATSINK FASTENER ON ASIC	5322 255 41211
ARALDIT GLUE 144-2/HV997	5322 390 50027

Give the glue 8 Hours to dry (at room temperature).

WARNING: HANDLE ARALDIT GLUE WITH CARE. AVOID CONTACT WITH EYES AND WASH HANDS CAREFULLY AFTER USE.

a) ***Removing an ASIC***

1. Remove the heatsink (if any) from the ASIC, using a TORX screwdriver.

2. Fit the required solder nozzle to the soldering tool, the size of the nozzle should be fractionally larger than that of the ASIC to be removed.

3. Power on the soldering tool with the temperature set to 5 on the scale and the air flow to maximum and let it heat up for approximately three minutes.

4. Apply a generous amount of flux to the pins of the target ASIC.

5. Position the board containing the component in a way that the ASIC is at approximately 85 degrees to the work surface and secure it, this position will allow the component to fall towards the iron when it becomes loose.

6. Position the nozzle around the ASIC at a distance of approximately 1 mm above the pins of the ASIC.

7. After a few seconds gently tap the ASIC with the wall of the nozzle to see if the ASIC is becoming de-soldered from the PCB, repeat this action until the ASIC is free.

8. Collect the ASIC in the mouth of the nozzle and quickly transfer the component to a safe place in order to cool.

NOTE: It is possible to carry out the above procedure with the PCB laid flat on the work surface. If this method is used the ASIC can be removed from the board when the solder has been melted by using a pair of tweezers. Care must be taken when using this method to ensure that none of the solder pads on the PCB are damaged.

WARNING: AT THIS STAGE OF THE OPERATION THE TEMPERATURE OF THE ASIC IS EXTREMELY HOT.

b) Cleaning the ASIC solder pads.

1. Place the PCB on a firm surface with the component side uppermost.

2. Apply a generous amount of flux to the solder connections that are to be cleaned.

3. Set the temperature of the soldering tool to 5 and the air flow to 2. Position the soldering nozzle approximately 1 mm above the surface of the solder pads and keep it in this position until the connections appear to be clean and there are no solder traces between adjacent pads.

4. Remove the soldering tool and examine the PCB carefully for any solder traces between adjacent pins.

5. Repeat procedures 2 - 4 as necessary.

c) Replacing the ASIC

1. Fit the pipe soldering nozzle to the soldering tool.

2. Adjust the heat setting on the soldering tool to five and the air flow to the middle of the range. This will prevent the flux and the ASIC being blown away.

3. Inspect the ASIC to be soldered to the PCB for pin damage, alignment and repair if necessary.

4. Position the replacement ASIC correctly on the PCB, using the notch on the corner of the ASIC as a reference point.

5. When the ASIC has been aligned correctly it must be made firm against the board to prevent slippage which in turn would cause bad connections to the pins. A recommended method is to use the metallic block. Place it on the centre of the ASIC, this would then have the dual purpose of a weight and a heat sink.

6. Apply a generous amount of flux to the pins of the ASIC.

7. Solder the pins of the ASIC to the PCB by gently going around the ASIC pin by pin with the pipe nozzle positioned about 5 mm above the solder pins.

CAUTION: Never add solder tin to the pins of the ASIC after it has been positioned as this could cause the solder to flow between the solder pads, if more solder is required to secure the ASIC it should be added to the pads on the PCB before positioning the ASIC.

6. After the completion of the operation confirm that all the pins have been soldered correctly by inspecting the area with a microscope.

9. If necessary, replace the heatsink on the ASIC, using the TORX screw.

7.2.3.3 Clock ASIC.

This ASIC does not have SMD pins and is soldered through the layers of the printed circuit board. You must **not** use a hot jet tool to remove this ASIC as doing so will cause damage to the board long before the ASIC is loose. It is recommended that a solder station comprising an in-built solder sucker and a high temperature soldering iron is used.

7.3 RE-CALIBRATION AFTER REPAIR.

After an input ASIC has been renewed the performance of that, and other closely related circuits, should be checked.
Refer to the performance analysis chapter in the service manual.

NOTES:

CHAPTER 8.

8. SPECIFICATION.

CONTENTS.

This chapter deals with the technical specifications of the PM 3580/PM 3585 Logic Analyzers.

The characteristics stated in this manual are based on the results of manufacturer's official checking procedures.
Details of these procedures and failure criteria will be supplied on request by the FLUKE/PHILIPS organization in your country, or by:

PHILIPS INTERNATIONAL B.V.
INDUSTRIAL ELECTRONICS, T&M DIVISION
SUPPLY CENTRE CUSTOMER SUPPORT DEPARTMENT
BUILDING TQIII-4
5600 MD EINDHOVEN
THE NETHERLANDS.

Properties expressed in numerical values with stated tolerance are guaranteed by the PHILIPS organization in your country.
Specified non-tolerance numerical values indicate those that could be nominally expected from the mean of a range of identical instruments.

The specifications are valid after the instrument has warmed up for at least 15 minutes.

Designation	Specification	Additional information

8.1 GENERAL CHARACTERISTICS.

8.1.1 DIMENSIONS.

- Height	220 mm (8.7")	}
- Width	420 mm (16.6")	} Excluding handle
- Depth	360 mm (14.2")	}

8.1.2. WEIGHT.

	13 kg (28.7 lbs)	Approx.

8.1.3 DISPLAY.

	9" monochrome	with 4 level greyscale

8.1.4. POWER.

- PM 3580	105 VA
- PM 3585	140 VA

8.2 ENVIRONMENTAL DATA.

8.2.1 STANDARDS.

MIL-T-28800 D, Type III,
Class 5, Style E.

8.2.2 TEMPERATURE.

- Rated Range of use	5°C to 40°C	(41°F to 104°F)
- Limited Range of operation	0°C to 55°C	(32°F to 131°F)
- Range for storage and transport	-40°C to 70°C	(-40°F to 158°F)

8.2.3 RELATIVE HUMIDITY.

- Operating	15% to 90%	non condensing
- Storage and transport	5% to 95%	non condensing

Designation	Specification	Additional information
8.2.4 ALTITUDE.		
- Operating	4500m	(15,000 ft)
- Storage and transport	12,000m	(40,000 ft)
8.2.5 VIBRATION.		
- Swept sine resonance search	5 - 55 Hz, 2g (peak) 15 min per axis, 10 min resonance dwell.	
8.2.6 EMI.		
	VDE 0871 Class B, FCC A	
8.2.7 SAFETY.		
	IEC 348 Class 1, VDE 0411, CSA 556 B.	

NOTE: These data do not apply to the disk media.

8.3 INPUT SECTION.

- Probe impedance	200 kΩ // 7 pF	Typical
- Thresholds per 8 channels	TTL, ECL or variable	 -3.0V to +12.0V. In 100 mV steps.
- Threshold accuracy	± 2.5% of V_{th}, ± 150 mV	V_{th} = selected threshold voltage
- Threshold overdrive	150 mV	
- Minimum swing peak to peak	2x (300 mV + 2.5% of V_{th}) Centred on V_{th}.	V_{th} = selected threshold voltage
- Maximum input voltage	± 50V	peak
- Channel to channel skew	< 4 ns	

Designation	Specification	Additional information

8.4 CONFIGURATIONS.

PM 3580 Analyzers have a single analyzer with dual-analysis-per-pin architecture. PM 3585 analyzers can be split into 2 logically separate analyzers. Each analyzer can be assigned any or all of the available 16 channel pods, and can acquire state and timing data on all channels simultaneously.

8.4.1 TIMING ANALYZER.

- Sample period			
PM 3580	10 ns		
PM 3585	5 ns		
- Sample period accuracy	0.005%		
- Time interval accuracy	± (One sample period + channel to channel skew + 0.005%) of the time interval reading.		
- Minimum detectable pulse			
PM 3580	11 ns	typical	
PM 3585	6 ns	typical	
PM 3580	12 ns	guaranteed	
PM 3585	7 ns	guaranteed	
- Storage method	Transitional		

8.4.2 GLITCH ANALYZER.

- Minimum detectable glitch	3 ns	typical
	4 ns	guaranteed

Designation	Specification	Additional information
8.4.3 STATE ANALYZER		
- Number of external clocks	4	Selectable from any channel. Clock Qualifier expressions defined by ANDing any/all input channels; up to 4 such expressions can de ORed together.
- Clock edges	Rising, falling or any	
- Minimum clock width	7 ns	
- Clock repetition rate	50 MHz	maximum
- Set up, hold time	Data and clock qualifiers must be present > 10 ns before, and remain present $\geq$ 0 ns after, the external clocking signal.	To support individual microprocessors, set-up and hold times are adapted as necessary to support the maximum processor speed.
- Max time-stamp error	$\pm$ (5 ns + 0.005% of time interval reading).	

Designation	Specification	Additional information

8.5 DATA MEMORY STORAGE MODES.

Data memory on the PM 3580 Family is separate from the timing memory. State date is always time-stamped.

NOTE: For Timing data length, minimum measurement length applies for signal rates > 25 MHz.
Maximum measurement length applies for very slow input signals.
Maximum time-correlated length of state data is 2 days.

- Timing/State		
PM 3580	512 states 5.12 μs to 6 hr Timing data length	Timing/State storage is default if an external clock is defined.
PM 3585	1024 states 5.12 μs to 12 hr Timing data length	
- State only		
PM 3580	1024 states	
PM 3585	2048 states	
- Timing only		Timing only storage is default if no external clock is defined.
PM 3580	10.24 μs to 12 hr Timing data length	
PM 3585	10.24 μs to 24 hr Timing data length	
- Timing/Glitch	5.12 μs to 12 hr Timing data length	
PM 3580	5.12 μs to 12 hr Timing data length	

Designation	Specification	Additional information

8.6 TRIGGER SEQUENCER.

Trigger sequencer for PM 3580 and for each logical analyzer in PM 3585. Note that all state and timing trigger recognizer's are always available, even when that data type is not being stored.

- sequence types	pre-defined, User-defined, Restart.
- Pre-defined sequences	Selection from standard list of commonly used sequences.
- User-defined sequences	8 trigger levels each of 2 trigger conditions (if, else if).
- Restart sequences	8 single condition trigger levels with global restart condition.
- Level to level delay	None
- Trigger conditions	Any ORed combination of either state or timing trigger recognizer, (NOT recognizer's are first ANDed) or time-out counter. On satisfying a condition, control is passed to any other trigger level.
- Acquisition halt	State or timing data acquisition can be independently halted or satisfying any trigger condition.

Designation	Specification	Additional information
- Counters	A total of 4 counters (1 to 65535) are available for use in any trigger condition as event or time-out counter.	

8.6.1 TRIGGER RECOGNIZER'S.

Each recognizer (except Glitch and Edge) uses an ANDed combination of bit values (0, 1 or X) for all defined labels.

8.6.1.1 Timing.

- Timing words	1 high speed word	(resolution = sample period + skew)
	2 width timing filters	(20 ns to 1.31 ms)
- Edge detector	Any ORed combination of any edges.	
- Glitch detector	Any ORed combination of glitches.	
- Glitch/Edge triggering	Isolated or during valid pattern which has been present for a minimum period	

Designation	Specification	Additional information
8.6.1.2 State.		
- State words	8 or 6 if timing filter words are used.	
- Range records	Range or NOT range	Range is defined as AND of range recognizer's for a number of labels. Up to 32-bits per label are allowed. Maximum 1 label per 16 channel group.
- Immediate recognizer's	Each pair of words can be used to recognize adjacent words	(w1:w2, w3:w4, etc.)
8.6.2 TIME-OUT COUNTER		
	20 ns to 65535 ms	
8.6.3 TRIGGER POSITIONS		
- Predefined positions	Beginning, Beginning + 25%, Centre, End - 25% or End, of acquired state and timing data.	Additionally, state and timing can each be arbitrarily delayed with respect to the trigger point in percent of memory, time (to a maximum of 65536 ms) or clocks (state only).
8.6.4 EXTERNAL TRIGGERING		
	Each trigger level can trigger and/or be triggered by an external instrument (via BNC) or the other logical analyzer in the PM 3585.	

Designation	Specification	Additional information

8.6.5 SELECTIVE STATE STORAGE

	Selective State Storage can be specified, either globally or per individual level, prior to the trigger point, using any ORed expression of the following: Anystate, Nostate, State word, NOT state word, Range, NOT range, Qualified external clock.	

8.7 ACQUISITION FUNCTIONS.

- Single	RUN key starts, Trigger sequencer or STOP key stops.	
- Auto-repeat	RUN key starts, Acquisition repeated indefinitely at programmed intervals.	
- Auto-repeat stop	Stop key, Compare/Non-compare	
- Auto-repeat delay	1s to 65535s	
- Status display	If the analyzer does not trigger within 1s of starting an acquisition, a status pop-up appears indicating the progression through the trigger levels.	Each acquisition is time stamped with the absolute time of the measurement (trigger point).

Designation	Specification	Additional information

8.8 LOGIC PROBING.

- Dynamic indication of signal status	High, Low or Changing	on all lines

8.9 LABEL FORMATTING AND ATTRIBUTES.

- Label names	Up to 8 character name defining signals or logical groups of signals (busses).	
- Maximum number of channels / labels	32	
- maximum number of labels	120	
- Label attributes	Validity for clocks, Inhibit timing data acquisition.	

8.10 DATA DISPLAY.

- Display modes	Single screen or dual screen	Each screen section can contain data of any type or source
- Data type	Timing waveform or state list	
- Data source	New measurement, Reference measurement or comparison of New and Reference measurements.	
- Display labels	Any labels defined in Format, displayed in any order.	Also time relative to trigger point and/or time-difference and clock (state lists).
- Level display	Current levels in trigger sequence are displayed.	

Designation	Specification	Additional information
- Measurement cursor's	R and S	
- Dial functions	Scroll, Set R-cursor, Set S-cursor, Set Time/division, Set vertical scale.	
- Dial mode	Movement on each dial-click: Scroll, Edge, Trigger level, Division, Page, Glitch Find pattern.	
- Find pattern (state)	Any bit-mask, defined by label.	
- Time/Division (timing)	3 steps per decade from 5 ns to 50 Ks	
- Co-scroll	Data in dual screen display can be scrolled synchronously with user-defined time-offset.	

8.11 DATA/SETTING STORAGE.

DOS format 2.0M-Byte (1.44M-Byte formatted) 3.5" floppy disk.	Will also accept externally formatted 720K-byte disks.

8.12 HARD-COPY OUTPUT.

Epson or Epson compatible printers via a Centronics parallel printer output.

Designation	Specification	Additional information

8.13 EXTERNAL VIDEO OUTPUT.

VGA compatible video output socket **(monochrome)**

8.14 EXTERNAL BNC TRIGGER.

- Active trigger level	High	
- Input resistance	100 kΩ	
- Minimum pulse width	25 ns	(typical)

8.15 EXTERNAL BNC TRIGGER OUT.

- Active trigger level	High	
- Output impedance	50Ω	
- Pulse width	20 ns	(typical)
- Delay between trigger condition true (at probe-tip) to trigger out true	approx. 430 ns	

CHAPTER 9.

9. SPARE PARTS.

CONTENTS.

9.1 UNITS & ASSEMBLIES.

REP. = This part is in the "REPAIRABLE (G2) PROCEDURE".

MAIN BOARD 296	COMPLETE	REP.	5322 214 90493
MAIN BOARD 264	COMPLETE	REP.	5322 214 90531
MAIN BOARD 164	COMPLETE	REP.	5322 214 90529
MAIN BOARD 132	COMPLETE	REP.	5322 214 90528

POWER SUPPLY UNIT	5322 218 51039
FLOPPY DRIVE 1.4 MBYTE	5322 693 22588
9" MONITOR (Complete, Boards included)	5322 218 61426
MONOCHROME TUBE M24-306WR/ED	5322 131 20404
KEYBOARD UNIT (Complete)	5322 693 91467
FAN + CABLE	5322 361 10576
MAINS ENTRY UNIT	5322 277 11235

9.2 MAIN BOARD PARTS.

9.2.1 ASIC's.

D1-D12	Input ASIC	5322 209 63401
D206	BOUNDARY SCAN ASIC (BA)	5322 209 51964
D5000-D5005	ACQUISITION ASIC (AA)	5322 209 62348
D5006 D5007	TIME ASIC (TA)	5322 209 62349
D5009 D5010	TIME ASIC (TA)	5322 209 62349
D5020 D5021	SEQUENCER ASIC (SA)	5322 209 62351
D6000	CLOCK ASIC (CA)	5322 209 62352

9.2.2 INTEGRATED CIRCUITS.

D100	SN74LS244DW	8x BUFF 3-ST	5322 209 62292
D101	MAX232CWE	2x RS-232	5322 209 62344
D102	SCC68070CAA84	16 BIT UP	5322 209 62199
D103	74F194SC	4 BIT SH REG	5322 209 62345
D105	SCC66470CAB	VIDEO SYST CTR	5322 209 62348
D110	PCF8583T	REAL TIME CLOCK	5322 209 62343
D120	74F00SC	4x 2-INP NAND	5322 209 72197
D130	74F139SC	2x 2-TO-4	5322 209 63862
D173	74F74SC	2x D-FF	5322 209 62291
D203	SN74LS244DW	8x BUFF 3-ST	5322 209 62292
D218 D219	PE21217LMD	DELAY LINE	5322 209 70202
D220 D221	SN74BCT8244DW	8x BUFF 3-ST	5322 209 62378
D303 D306	74F245SC	8x BUS TRANSC	5322 209 62293
D304 D307	SN74LS374DW	8x D-FF	5322 209 73969
D320 D321	SN74BCT8245DW	8x BI-DIR BUF	5322 209 62379
D400 D403	D27C512-150V10	EMPTY EPROM	5322 209 12445
D400	BOOT PROM EVEN	(PROGRAMMED)	5322 209 51942
D401 D402	HM62256LFP-12T	32K x 8 SRAM	4822 209 63215
D403	BOOT PROM ODD	(PROGRAMMED)	5322 209 51941
D404 D405	HM62256LFP-12T	32K x 8 SRAM	4822 209 63215
D406	GAL	SRAM SELECT	5322 209 63407
D500	GAL	FDC CONTROL	5322 209 63408
D501	DP8473V	FLOPPY CONTROL	4822 209 63212
D600	GAL	DTACK CONTROL	5322 209 63409
D601	MC68901FN	MULTIFUN.PERIP	5322 209 62377
D802 D603	PE21217LMD	DELAY LINE	5322 209 70202
D700	SN74LS244DW	8x BUFF 3-ST	5322 209 62292
D701	MC68230P8	PARALLEL PORT	5322 209 60892
D702	SN74LS244DW	8x BUFF 3-ST	5322 209 62292
D703	GAL	!/OSELECT	5322 209 63411
D802	GAL	!/ODATACONTROL	5322 209 63412
D1000-D1007	HM514256AP-10	256K x 4 DRAM	5322 209 62374
D1020-D1023	HM514256AP-10	256K x 4 DRAM	5322 209 62374
D6001	MC10E111FN	CALIBR. DRIVER	5322 209 62376
D6002	MC10H210FN	DUAL 3-INP OR	5322 209 62375
D6003	MC10124FN	4x TTL/ECL CONV	4822 209 63213
D7000	PC74HCT240T	8x BUFF INV	4822 209 63214
D7001	PC74HCT02T	4x 2-INP NOR	5322 209 11595

9.2.3 XTALS.

G2	CRYST.OSCILL. 200MHZ	5322 242 73588
G100	XTAL TO5300-30M	5322 242 73592
G101	XTAL TO5330-19M6608	5322 242 73852
G102	CRYST.OSC. MCO14258-4M9152	5322 242 73853
G104	XTAL 32.768 KHz	5322 242 73682
G500	XTAL TO5330-24M	5322 242 73851
G700	CRYST.OSCILL. MCO1425B-8M	5322 242 73854

9.2.4 SEMI-CONDUCTORS.

V100 V101 V103	SCHOTTKY DIODE BAT85	4822 130 31983
V105 V106	SCHOTTKY DIODE BAT85	4822 130 31983
V701 V702	SCHOTTKY DIODE BAT54	4822 130 80622
V7000-V7003	SCHOTTKY DIODE BAT85	4822 130 31983
V102 V104 V700	SWITCH TRANS PH2369	4822 130 41594

9.2.5 CAPACITORS.

C100	Elcap 10V 22UF	5322 124 11193
C101 C102	Elcap 16V 22UF	5322 124 11195
C105 C106	Elcap 16V 22UF	5322 124 11195
C109	Trim Cap. 250V 22PF	4822 125 50045
C176 C900 C901	Elcap 10V 47UF	5322 124 11194
C8100 C8200	Elcap 16V 4.7UF	5322 124 11018
C8226 C8239	Elcap 16V 4.7UF	4822 124 11018
	Cer. Cap. 63V 3.9PF	4822 122 32081
	Cer. Cap. 63V 5% 10PF	4822 122 31971
	Cer. Cap. 63V 5% 22PF	4822 122 32482
	Cer. Cap. 63V 10% 47PF	4822 122 31772
	Cer. Cap. 63V 10% 100PF	4822 122 31765
	Cer. Cap. 63V 10% 220PF	4822 122 31965
	Cer. Cap. 63V 10% 1NF	4822 122 31746
	Cer. Cap. 40V 10NF	4822 122 30043
	Cer. Cap. 63V 10% 22NF	4822 122 31797
	Cer. Cap. 63V 10% 27NF	4822 122 32541
	Cer. Cap. 63V 10% 47NF	4822 122 32542
	Cer. Cap. 63V 10% 100NF	4822 122 33104

9.2.6 RESISTORS.

	RES CHIP RC-01 5% 33E	4822 051 10339
	RES CHIP RC-01 5% 47E	4822 051 10479
	RES CHIP RC-01 5% 68E	4822 051 10689
	RES CHIP RC-01 5% 91E	4822 051 10919
	RES CHIP RC-01 5% 100E	4822 051 10101
	RES CHIP RC-01 5% 120E	4822 051 10121
	RES CHIP RC-01 5% 150E	4822 051 10151
	RES CHIP RC-01 5% 560E	4822 051 10561
	RES CHIP RC-01 5% 1K	4822 051 10102
	RES CHIP RC-01 5% 2K2	4822 051 10222
	RES CHIP RC-01 5% 2K7	4822 051 10272
	RES CHIP RC-01 5% 3K3	4822 051 10332
	RES CHIP RC-01 5% 4K7	4822 051 10472
	RES CHIP RC-01 5% 5K6	4822 051 10562
	RES CHIP RC-01 5% 10K	4822 051 10103
	RES CHIP RC-01 5% 100K	4822 051 10104
	RES CHIP RC-02G 1% 316E	4822 116 81789
	RES CHIP RC-02G 1% 2K61	4822 111 91821
	RES CIRC 1% 20K	5322 111 91911
R104	BOUR CIRC 4608X-102-220 22E	5322 111 91482
R130	INTENSITY POTM 0.2W 20% 1M	5322 101 21106
R179	METAL FILM RES. 121K 1%	4822 050 21214
R599	BOUR CIRC 4606X-101-151 150E	5322 111 91926
R900 R901	BOUR CIRC 4610X-105-102 1K	5322 111 90463
R903-R908	BOUR CIRC 4610X-104-220E/330E	5322 111 90833
R6014	BOUR CIRC 4610X-105-151 150E	5322 111 91171
R6015	BOUR CIRC 4610X-105-101 100E	5322 111 91169
R7000-R7007	METAL FILM RES. 383E 1% 0.6W	4822 050 23831
R8000-R8003	WIRE WOUND RES. 6E8 10% 5.8W	4822 112 41049

9.2.7 CONNECTORS.

X1-X6	INPUT POD CONNECTOR 40-P	5322 401 11036
X100	RS232 OUTPUT PORT CONN. 25-P	5322 265 51289
X101	KEYBOARD INPUT CONN. 4-P	5322 265 30811
X102	VIDEO OUTPUT CONN. 10-P	5322 266 51022
X103	MVGA OUTPUT CONN. 15-P	5322 267 51056
X104	VIDEO DISPLAY BACKGROUND 3-P	5322 265 30898
X105	RESET CPU PART 2-P	5322 285 20521
X402	EPROM TYPE SELECTION 3-P	5322 265 30878
X500	SELECT EXTERN. DATA SEP. 2-P	5322 285 20521
X501	DRIVE CTRL SIGNALS TYPE 2-P	5322 265 20521
X502	FLOPPY DRIVE CONN. 34-P	5322 267 70174
X700	CENTRONIX PAR. OUTPUT 25-P	5322 267 60287
X701	BST CONN. (EXTERNAL) 5-P	5322 265 30779
X702	BEEPER CONNECTOR 2-P	5322 265 20521
X703 X704	HARDWARE BOARDTYPE SELECT 2-P	5322 285 20522
X705	CHIP SELECT PROM CONN. 2-P	5322 265 20521
X800	IEEE CONNECTOR 24-P	5322 287 60162
X801	IEEE TRANSMIT/RECEIVE DIS 2-P	5322 265 20521
X900	POWER SUPPLY CONN. 14-P	5322 265 41026
X902	FAN UNIT CONNECTOR 2-P	5322 265 20486
X5001-X5003	BST CHAIN JUMPERS 2-P	5322 265 20521
X7000	BNC TRIGGER OUT	5322 267 10004
X7001	BNC TRIGGER IN	5322 267 10004

9.2.8 MISCELLANEOUS.

F902-F905	MULTIFUSE OVERCURR. PROT	5322 252 11104
G110	LITH BATTERY BR-2/3A-1P (NON CHARGEABLE)	5322 138 10263
L104 L910	MICRO CHOKE 10UH	5322 157 53393
L100 L911	WND 6-H BEADS 50MC	5322 158 10052
L900-L906	WND 6-H BEADS 50MC	5322 158 10052
L700-L713	CHIP INDUCTOR 10UH	4822 157 53904
S7010-S7012	THERMO-SWITCH 70 C NO	5322 277 11234
	CHIP HOLDER 84-P FOR D102	5322 255 40823
	IC SOCKET DIL 32-P	4822 255 40921
	IC SOCKET DIL 40-P	5322 255 44217
	IC SOCKET DIL 20-P	5322 255 40425
	HEATSINK FASTENER ON ASIC	5322 255 41211
	HEATSINK FOR ASIC	5322 255 41212
	ARALDIT GLUE 144-2/HV997	5322 390 50027

9.3 MONITOR.

9.3.1 CONTROL BOARD PARTS.

R1	MRS16T 681K	4822 050 16814
R2	PRO1 100E	4822 053 10101
R3	NFR25 5E6 5%	4822 052 10568
R4	PRO1 47K	4822 053 10473
R5	SFR16T 2E2	4822 116 81154
R6	MRS16T 348K	4822 050 13484
R7	MRS16T 100K	4822 050 11004
R8	MRS16T 56K2	4822 050 15623
R9	SFR16T 1E	4822 116 80176
R10	SFR16T 3K9	4822 116 52276
R11	SFR16T 47K	4822 116 52284
R12	MRS16T 36K0	4822 050 13603
R13 R14 R37	SFR16T 4K7	4822 116 52283
R15 R18	SFR16T 100E	4822 116 52175
R17	SFR16T 470E	4822 116 52224
R18	PRO1 56E	4822 053 10569
R19	SFR16T 560E	4822 118 52226
R20	SFR16T 270E	4822 116 52217
R21 R25	SFR16T 100E	4822 116 52175
R22	SFR25H 1K	4822 050 21002
R23	SFR16T 1K	4822 116 52204
R24	PRO2 1E	4822 053 11108
R26	PRO2 330K	4822 053 11334
R27	SFR16T 680K	4822 116 52298
R28	SFR16T 220K	4822 116 52258
R29	VR25 2M2	4822 110 72196
R30	SFR16T 180K	4822 116 52252
R31	SFR16T 22K	4822 116 52257
R32 R33	SFR16T 10K	4822 116 52233
R34	SFR16T 330E	4822 116 52219
R35	SFR16T 390K	4822 116 52278
R38	SFR16T 5K6	4822 116 52289

C1 C7	CAP 220NF 63V 10%	4822 121 41741
C2 C20	ELCO 150UF 16V 20%	4822 124 40195
C3 C8	ELCO 1000UF 10V	4822 124 22496
C4	ELCO 47UF 25V 20%	4822 124 40433
C5	CAP 100NF 100V 10%	4822 121 41853
C6 C9	CAP 22NF 100V 10%	4822 121 41934
C10 C28	ELCO 1UF 63V 20%	4822 124 40242
C11 C27	KERCO 4.7NF 10% 100V	4822 122 30128
C12	CAP 1000PF 400V 10%	4822 122 40396
C13 C26	KERCO 680PF 10% 100V	5322 122 32052
C14	ELCO 22UF 63V 20%	4822 124 40804
C15	CAP 33NF 100V 10%	4822 121 43104
C16	CAP 5800PF 630V 5%	5322 121 43687
C17	KERCO 330PF 10% 500V	4822 122 31165
C18	CAP 0.47UF 100V 5%	5322 121 41533
C22	ELCO 10UF 63V 20%	4822 124 40248
C23	CAP 10NF 400V 10%	4822 121 41677
C24	KERCO 1NF 10% 500V	5322 122 32127
C25	KERCO 1NF 10% 100V	5322 122 32331
P1	TRIMMER 100E(VERTICAL SIZE)	5322 101 11075
P2	TRIMMER 1M (FOCUS)	4822 100 11022
D1	BAX18	4822 130 34121
D2 D7	BAW62	4822 130 30613
D3	BYD33J	4822 130 42606
D4	BYD74G	4822 130 81175
D5	BAV21	4822 130 30842
D6	BYD33M	4822 130 32896
O1	BC640	4822 130 41078
O2	MJE13009	5322 130 62705
O3	BUX87	5322 130 44918
O4	BC548	4822 130 41001
T1	LINE TRAFO AT2140/17	5322 140 10419
T2	DRIVER TRANSFORMER AT4043/89	4822 150 50051
U1	PULSE WIDTH MODULE TEA2037A	4822 209 63819

9.3.2 CRT BOARD PARTS.

R101	39K 0.6W 1%	4822 050 23903
R102	100K 0.6W 1%	4822 050 21004
R103	NFR25H 3E3 5%	4822 052 11338
R104	470E 0.6W 1%	4822 050 24701
R105	PRO2 1K	4822 053 11102
R106	SFR16T 100E	4822 116 52175
R107	SFR16T 68E	4822 116 52199
R108	MRS16T 91E	4822 050 19109
R109	MRS16T 47E	4822 050 14709
R110	SFR16T 470E	4822 116 52224
C101 C102	CAP 0.1UF 10% 400V	4822 121 42059
C103	ELCO 47UF 63V 20%	4822 124 41069
C104	ELCO 150UF 16V 20%	4822 124 40195
C105	KERCO 22PF 2% 100V	5322 122 32143
C106 C107	KERCO 4.7NF 10% 100V	4822 122 30128
J102	CRT SOCKET	5322 255 41138
Q101	BC546	4822 130 41001
Q102	BC549C	4822 130 44246

9.4 POWER SUPPLY PARTS.

D1 D2	FR107	5322 130 82414
D7	SF164C	5322 130 82417
D8	ESAD83-004	5322 130 82413
D9	SF164A	5322 130 82416
D10 D11 D12	1N4148	4822 130 30621
DB1	RS605	5322 130 82415
DB2 DB3	DB101	5322 130 82412
IC1	TL494CN	5322 209 81106
IC2	LM7905CT	4822 209 62912
Q1 Q2	2SC2625-33	4822 130 62431
Q3 Q4	VN10KM FET	5322 130 42516
Q5 Q6 Q7	2SA1015	4822 130 41505
Q8	2SC1815	4822 130 41306
Q9 Q10 Q12	2SA1015	4822 130 41505
Q11	2SC1815	4822 130 41306
Q13 Q14	2SD1062	5322 130 62545
THSW1	THERMOSWITCH 9OP72 85°C	5322 282 50096

9.5 KEYBOARD UNIT PARTS.

D1	MAB8401B	5322 209 11719
D1	PROGRAMMED EPROM	5322 209 51974
G1	XTAL TO5330-6M	5322 242 73687
S99	ROTARY DIAL UNIT	5322 273 80345
	DIAL KNOB FOR S99	5322 414 30178

9.6 GENERAL PARTS.

INTENSITY CONTROL KNOB FOR R130		5322 414 30182
FUSE 5 X 20	2A SLOW	4822 070 32002
FUSE 5.2 X 20	4A SLOW	4822 253 30028
FRONT WALL		5322 447 91781
REAR WALL		5322 447 91782
COVER		5322 447 91785
FOOT		5322 462 41673
LOGO PM 3580 100 MHZ		5322 456 90438
LOGO PM 3585 200 MHZ		5322 456 90439
HANDLE ASSEMBLY		5322 498 50313
STOP DISK OF HANDLE ASSEMBLY (SEE CHAPTER 2)		5322 466 92997
HANDLE SIDE COVER (SEE CHAPTER 2)		5322 600 30047
KEYBOARD CABLE	(TO MAINBOARD)	5322 321 60624
MONITOR CABLE	(TO MAINBOARD)	5322 321 60626
POWER SUPPLY CABLE	(TO MAINBOARD)	5322 321 10747
FLOPPY POWER CABLE	(FILTER UNIT TO DRIVE)	5322 321 60625
FLOPPY DATA CABLE	(FILTER UNIT TO DRIVE)	5322 321 60627
FLOPPY CABLE	(MAINBOARD TO FILTER UNIT)	5322 321 61218
FLOPPY DRIVE FILTER UNIT		5322 480 20129
TORX TAPTITE SCREW M2.5 x 6		4822 502 13172
TORX M3 x 6		4822 502 11667
TORX M4 x 12		4822 502 11686

9.7 ADAPTORS.

8085	DIP-CLIP ADAPTOR	5322 214 90667
6800	DIP-CLIP ADAPTOR	5322 214 90669
6809	DIP-CLIP ADAPTOR	5322 214 90671
Z80	DIP-CLIP ADAPTOR	5322 214 90668
8051	DIP-CLIP ADAPTOR	5322 214 90672
68HC11	PLCC ADAPTOR	5322 214 90677
68000	DIP-CLIP ADAPTOR	5322 214 90682
68000	DIP-SOCK ADAPTOR	5322 214 90663
68000	PLCC-SOCK ADAPTOR	5322 214 90664
88000	PGA ADAPTOR	5322 214 90665
8086/88	DIP-CLIP ADAPTOR	5322 214 90673
80186	PGA ADAPTOR	5322 214 90674
00286	PLCC ADAPTOR	5322 214 90678
80286	PGA ADAPTOR	5322 214 90675
80186/88-EB	PLCC ADAPTOR	5322 214 90679
68020	PGA ADAPTOR	5322 214 90666
386DX	PGA TIMING ADAPTOR	5322 214 90676
80486	PGA TIMING ADAPTOR	5322 214 90682
80960CA	PGA TIMING ADAPTOR	5322 214 90681
6502	DIP-CLIP ADAPTOR	5322 214 90777
8051	DIP-CLIP ADAPTOR	5322 214 90778
64180	PLCC-SOCKET ADAPTOR	5322 214 90775
80515	PLCC-SOCKET ADAPTOR	5322 214 90776
68HC11F	PLCC ADAPTOR	5322 214 90779
MCS-96	PLCC ADAPTOR	5322 214 90773
68030	PGA ADAPTOR	5322 214 90771
386DX	PGA ACTIVE ADAPTOR	5322 214 90769
I486	PGA ACTIVE ADAPTOR	5322 214 90774
I960CA	PGA ACTIVE ADAPTOR	5322 214 90772

NOTE: These adaptors are in the 'repairable (G2) procedure'.

9.8 TEST EQUIPMENT.

RS-232-C LOOP BACK TEST ADAPTOR	5322 693 91481
CENTRONICS DIODE MATRIX CONNECTOR	5322 693 91479
EXTENSION CABLE FOR THE VDU	5322 321 61069
EXTENSION CABLE FOR THE KEYBOARD	5322 321 61068
PM358X BST & DIAGNOSTIC TEST DISKS	5322 310 10493

NOTES:

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